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FORM PTO-1390 (REV. 12-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY 'S DOCKET NUMBER: OGOH:106

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 10/070554

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/06173	8 September 2000	8 September 1999

TITLE OF INVENTION: ELECTRICAL CIRCUIT BOARD AND TFT ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME

APPLICANT(S) FOR DO/EO/US: Kazufumi OGAWA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [x] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [x] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [x] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [x] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [x] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [x] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [x] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [x] Other items or information:
   Application Data Sheet;
   International Application Publication Cover Page;
   PCT Request;
   Forms PCT/IB/301; 304; 308 and 332.

PLEASE ACCEPT THIS AS AUTHORIZATION TO DEBIT OR CREDIT FEES TO DEP. ACCT. 16-0331 PARKHURST & WENDEL

10070554.030702

JC19 Rec'd PCT/PTO 07 MAR 2002

U.S. APPLICATION NO. (if known, see 37 CFR 1.5) 10/070554	INTERNATIONAL APPLICATION NO. PCT/JP00/06173	ATTORNEY'S DOCKET NUMBER OGOH:106

	CALCULATIONS	PTO USE ONLY
21. [X] The following fees are submitted: **BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):** Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO . . . . **$1040.00** International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO . . . . **$890.00** International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO . . . . **$740.00** International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) . . . . **$710.00** International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	101 - 20 =	81	x **$18.00**	$ 1,458.00	
Independent claims	26 - 3 =	23	x **$84.00**	$ 1,932.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$	
TOTAL OF ABOVE CALCULATIONS =				$ 4,280.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +				$	
SUBTOTAL =				$ 4,280.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$	
TOTAL NATIONAL FEE =				$ 4,280.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 4,320.00	
				Amount to be refunded:	$
				charged:	$

a. [X] A check in the amount of $ 4,320.00 to cover the above fees is enclosed. CK# 15131

b. [ ] Please charge my Deposit Account No. ______________ in the amount of $ __________ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 160331 . A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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~~25,177~~ 24,453
REGISTRATION NUMBER

10070554 .030702

10/070554

JC19 Rec'd PCT/PTO 07 MAR 2002

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Kazufumi OGAWA

Serial No.: New Application

Filed: March 7, 2002

For: ELECTRICAL CIRCUIT BOARD AND TFT ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-identified application, please enter the following specification changes as noted below:

IN THE SPECIFICATION:

Page 2, second paragraph, cancel and replace with:

(1) A first aspect of the present invention (first to seventh embodiments) for achieving this object relates to a structure for

electrical circuit boards applicable to semiconductor integrated circuits and the like. The first aspect of the present invention includes the following.

Page 4, second full paragraph, cancel and replace with:

(2) A second aspect of the present invention (eighth to eighteenth embodiments) relates to a bottom-gate TFT array substrate to which the above-described electrical circuit board is applied, and includes the following.

Page 6, line 20 to Page 7, line 25, cancel and replace with:

Specifically, the method comprising: (A) sequentially depositing at least a G-S metal film layer, a gate insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines; (B), after step (A), by photolithography, using a first resist pattern, etching the layers through to the surface of the insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section

pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines; (C), after step (B), oxidizing side surfaces of the gate electrodes and side surfaces of the gate wiring lines to form an electrically insulating metal oxide film; (D), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and (E), after step (D), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a

predetermined pattern to form pixel electrodes and etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form channel regions on the semiconductor film.

Page 8, lines 1 to 14, cancel and replace with:

In this fabrication method, the oxidation of the side surfaces of the gate electrodes and the side surfaces of the gate wiring lines may be carried out by anodic oxidation.

In addition, the semiconductor film layer may have a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and step (E) of etching the contact metal film of the gate electrode section pattern may be carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous silicon layer.

Furthermore, in place of the transparent conductive film layer in step(D), a light reflective conductive film layer may be deposited.

(3) A third aspect of the present invention (nineteenth to twenty-third embodiments) relates to a liquid crystal display device utilizing a bottom-gate TFT array substrate, and includes the following.

Page 10, lines 1 to 21, cancel and replace with:

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the reflective pixel metal electrodes has a two-layered structure composed of a contact electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode.

(Twenty-fifth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the reflective pixel metal

electrode group is one selected from the group consisting of aluminum and an aluminum-based alloy.

(Twenty-sixth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that part of each source segmented wiring line has a two-layered structure composed of a contact metal film and an aluminum-based metal electrode film.

Page 10, line 23 to Page 11, line 7, cancel and replace with:

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the gate insulating film and the semiconductor film are formed between the gate electrode metal and the contact electrode metal.

(Twenty-eighth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact electrode metal and the metal electrode.

Page 11, line 19, to Page 12, line 3, cancel and replace with:

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact metal film, and the semiconductor film, using a second pattern.

Page 12, line 21, to Page 13, line 11, cancel and replace with:

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each

having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode; and a color filter substrate having a color filter side on which a counter transparent electrode is formed; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

Page 13, line 23, to Page 14, line 16, cancel and replace with:

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially

etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact metal film, and the semiconductor film, using a second pattern; forming an alignment film on the first substrate; forming an alignment film on a surface of a counter electrode side of a second color filter substrate having a counter transparent electrode formed thereon; adhering and fixing the first and second substrates and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

Page 14, lines 23 to 25, cancel and replace with:

The fabrication method according to the thirty-ninth embodiment may be such that the metal electrode and the contact electrode metal are formed in a single layer with a same material.

Page 15, lines 4 to 13, cancel and replace with:

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized; each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

Page 15, lines 20 to 24, cancel and replace with:

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the first comb-shaped pixel electrodes and part of each source segmented wiring line have a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact metal film layer, and a metal electrode film.

Page 16, line 22, to Page 17, line 7, cancel and replace with:

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern.

Page 19, lines 2 to 19, cancel and replace with:

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by

photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; forming an alignment film on the first substrate; forming an alignment film on a surface of a second color filter substrate; adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

Page 19, line 21, to Page 20, line 2, cancel and replace with:

The fabrication method according to the fifty-seventh embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a

passivation film; and using the passivation film as a mask, etching the metal electrode film, the contact metal film layer, the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

Page 20, lines 9 to 19, cancel and replace with:

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode.

Page 21, lines 1 to 16, cancel and replace with:

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact metal film layer, and a metal electrode film.

(Sixty-third embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that the contact electrode metal is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

(Sixty-fourth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact electrode metal and the metal electrode.

Page 22, lines 3 to 13, cancel and replace with:

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact metal film layer and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern.

Page 23, lines 8 to 22, cancel and replace with:

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a

contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

Page 24, line 9, to Page 25, line 1, cancel and replace with:

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be

formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact metal film layer and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; forming an alignment film on the first substrate; forming an alignment film on a surface of a counter electrode side of a second color filter substrate; adhering and fixing the first and second substrates and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

Page 25, lines 8 to 25, cancel and replace with:

The fabrication method according to the seventy-fifth embodiment may be such that the metal electrode and the contact electrode metal are formed in a single layer with a same material.

(16) A sixteenth aspect of the present invention (seventy-eighth to eighty-fourth embodiments) includes the following.

(Seventy-eighth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and the second comb-shaped pixel electrodes are formed with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate.

Page 26, lines 6 to 10, cancel and replace with:

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate insulating film, a semiconductor film, a contact metal film layer, and a metal electrode film.

Page 27, lines 8 to 20, cancel and replace with:

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped pixel electrodes using a third pattern with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate.

Page 28, line 14, to Page 29, line 4, cancel and replace with:

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the

gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped pixel electrodes formed with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

Page 29, line 16, to Page 30, line 10, cancel and replace with:

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by

photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate; forming an alignment film on the first substrate; forming an alignment film on a surface of a color filter side of a second color filter substrate; adhering and fixing the the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

Page 30, lines 12 to 15, cancel and replace with:

The fabrication method according to the ninety-third embodiment may further comprise, after the formation of the second comb-shaped pixel electrodes, covering at least part of each second comb-shaped pixel electrode by a passivation film.

Page 30, line 22, to Page 31, line 8, cancel and replace with:

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal; each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and the second comb-shaped pixel electrodes are formed with a passivation film disposed between the second-comb shaped pixel electrodes and the substrate.

Page 31, line 17, to Page 32, line 4, cancel and replace with:

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact metal film layer and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate.

Page 32, lines 8 to 23, cancel and replace with:

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at

least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped pixel electrodes formed with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

Page 33, lines 3 to 21, cancel and replace with:

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal

film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact metal film layer and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate; forming an alignment film on the first substrate; forming an alignment film on a surface of a color filter side of a second color filter substrate; adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

Page 33, lines 23 to 24, cancel and replace with:

The fabrication method may further comprise covering at least part of each second comb-shaped pixel electrode by a passivation film.

Page 41, lines 17 to 25, cancel and replace with:

Subsequently, a second resist pattern 208′ for the second photolithography (Figs. 10(a) and 10(b)) was formed by a conventional method. Then, part of the transparent conductive film 212, the contact metal film 207′, and the n+a-Si film 206′ on the gate electrode were sequentially etched away through to the i-type a-Si film 205′, thus forming channel regions. The source segmented wiring line 209′ was connected to a source region 213 by a portion of the contact electrode 207′ and a transparent conductive film 214, and the pixel transparent electrode 215 was connected to a drain region 216 by a portion of the contact electrode 207′ (Figs. 11(a) and 11(b)).

Page 42, lines 5 to 16, cancel and replace with:

Finally, by using printing and baking a silica passivation film layer 217 of 300 nm was formed on the substrate, except for the periphery thereof, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, the peripheral portion of the stacked layers of the i-type a-Si film 205 and the gate insulating film layer 204 (SiN_x film), which is to be connected to external driving circuitry, was etched away to expose the gate G-S metal film 203 (see Fig. 11). Thereby, a TFT array substrate 218 (Fig. 26) applicable to transmissive liquid crystal display devices was produced.

Fig. 12 is an enlarged schematic plan view of a main portion of the TFT array substrate 218 produced in the present example. Fig. 11(a) is a cross-sectional view taken along the line A-A′ of Fig. 12, and Fig. 11(b) is a cross-sectional view taken along the line B-B′ of Fig. 12.

Page 43, lines 18 to 21, cancel and replace with:

In this example, the source segmented wiring lines have a five-layered structure composed of the G-S metal film, a gate insulating film, the semiconductor film, the contact metal film, and the conductive film, and therefore the overall resistance of the source segmented wiring lines is reduced.

Page 44, line 18, to Page 45, line 1, cancel and replace with:

First, there were provided a TFT array substrate, similar to that of Example 2-1, fabricated using two masks, more specifically, a first TFT array substrate 223 including a first electrode group 221 arranged in a matrix and a transistor group 222 that drives the first electrodes; and a second color filter substrate 226 including a second electrode 225 and a color filter group 224 placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 227.

Page 46, lines 16 to 21, cancel and replace with:

Thereafter, the n+a-Si film layer 206, the i-type a-Si film layer 205, the gate insulating film layer 204 (SiN_x film), and the G-S metal film layer 203 (Al-Zr film) were sequentially etched, thereby forming a first pattern 240 including a gate electrode 203′ or a gate wiring line 203″, a source segmented wiring line 209′, a gate insulating film 204′, and a semiconductor film (205′+206′) which were stacked (Figs. 15(a) and 15(b)).

Page 46, line 22, to Page 47, line 7, cancel and replace with:

Then, the gate electrode 203′ and the gate wiring line 203″ were anodically oxidized in an electrolyte to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the gate electrode and the side surfaces of the gate wiring line (Figs. 16(a) and 16(b)). Thereafter, a contact metal film (Ti) 241 and a metal electrode film 242 composed of an aluminum film (Al) were vapor deposited by sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact metal film and the metal electrode film were to be connected to pixel metal electrodes connected to drain regions and were to connect together segments of

each severed source segmented wiring line connected to source regions (Figs. 17(a) and 17(b)).

Page 47, line 8, to Page 48, line 1, cancel and replace with:

Subsequently, a second resist pattern 208′ for the second photolithography was formed by a conventional method (Figs. 18(a) and 18(b)). Then, part of the metal electrode film 242, the contact metal film (Ti) 241, and the n+a-Si film 206′ on the gate electrode were sequentially etched away, thus forming channel regions, The source segmented wiring line 209′ was connected to a source region 213 by a portion of a contact metal film (Ti) 241′ and a metal electrode film pattern 242′, and a pixel metal electrode film 243 was connected to a drain region 216 by the contact electrode metal 241′ (Figs. 19(a) and 19(b)). At this point, segments of the source segmented wiring line 209′, which had been previously severed and disconnected, were connected together on the gate wiring line 203″ by the portion of the contact metal film (Ti) 241′ and the metal electrode film pattern 242′ (Fig. 19(b)).

Finally, by using printing and baking a silica passivation film 217 of 300 nm was formed on the substrate, except for the periphery

thereof, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal, which are to be connected to driving circuitry, were etched away, thus producing a TFT array substrate 245 having reflective pixel metal electrodes in the pixel portions (Figs. 20(a) and 20(b)).

Page 48, lines 2 to 5, cancel and replace with:

According to the present example, segments of each source segmented wiring line are connected together by the two layers of the contact electrode metal and the metal electrode, and therefore the resistance of the source segmented wiring lines was made extremely low.

Page 48, lines 21 to 25, cancel and replace with:

In addition, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact metal film, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring lines.

Page 49, lines 1 to 9, cancel and replace with:

Forming the silicon nitride-based gate insulating film and the semiconductor film between the gate electrode metal and the contact electrode metal made it possible to fabricate a TFT array substrate having excellent stability.

When segments of each source segmented wiring line, which had been severed by the gate wiring lines, were interconnected together on the gate wiring lines by the two layers of the contact electrode metal and the metal electrode, it was possible to minimize level differences on the surface of the TFT array substrate.

Page 49, line 21, to Page 50, line 4, cancel and replace with:

First, there were provided a TFT array substrate, similar to that of Example 2-3, fabricated using two masks, more specifically, a first TFT array substrate 323 including a first electrode group 321 arranged in a matrix and a transistor group 322 that drives the first electrodes; and a second color filter substrate 326 including a second electrode 325 and a color filter group 324 placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and

the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 327.

Page 50, line 15 to Page 51, line 5, cancel and replace with:

In a manner similar to that described in Example 2-1, a transparent glass substrate that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer, was deposited by CVD to 0.4 microns. Then, an Al-Zr (97:3) alloy, serving as a G-S metal film layer for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film layer not containing impurities and an amorphous silicon (n+a-Si) film layer containing an n-type impurity to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Page 51, lines 6 to 17, cancel and replace with:

Then, the contact metal film layer (Ti), the n+a-Si film layer, the i-type a-Si film layer, the gate insulating film layer (SiN_x film), and the G-S metal film layer (Al-Zr film) were sequentially etched, thereby forming a first pattern including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, and a semiconductor film, which were stacked, and a first comb-shaped pixel metal electrode 251.

Next, the gate electrode, the gate wiring line, and the first comb-shaped pixel metal electrode 251 were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Page 51, line 23, to Page 52, line 5, cancel and replace with:

Subsequently, a second resist pattern for the second photolithography was formed by a conventional method. Then, part of the metal electrode film, the contact electrode metal, and the n+a-Si film 206′ on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. The source segmented wiring line 209′ was connected to a source

region by a portion of the contact electrode metal and a metal electrode, and a second comb-shaped pixel metal electrode was connected to a drain region by a portion of the contact electrode metal.

Page 52, lines 6 to 16, cancel and replace with:

At this point, the source segmented wiring lines and, which had been previously severed, were connected together on the gate wiring line by the metal electrode film pattern via a portion of the contact electrode metal.

Finally, by using printing and baking a silica passivation film 217 of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the i-type a-Si film and the SiN_x film on the gate electrode metal, which are to be connected to external driving circuitry, were etched away, thus producing a TFT array substrate 253 applicable to in-plane switching (IPS) mode liquid crystal display devices (Figs. 22(a) and 22(b)).

Page 53, lines 3 to 11, cancel and replace with:

In the oxidation step, carrying out anodic oxidation in a neutral electrolyte made it possible to selectively oxidize and insulate only the side surfaces of the gate electrodes, the side surfaces of the gate wiring lines, and the side surfaces of the first comb-shaped pixel electrodes.

When the first comb-shaped pixel electrodes and part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact metal film layer, and the metal electrode film, it was possible to provide a TFT array substrate having little resistance of the source segmented wiring line.

Page 54, lines 7 to 23, cancel and replace with:

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-5, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the second comb-shaped electrode group; and a color filter substrate including a second color filter substrate group placed

opposite to the first and second electrodegroups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns created by spacers and adhesives. Thereafter, a nematic liquid crystal was injected between the first and second substrates, and polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Page 55, line 20, to Page 56, line 7, cancel and replace with:

In a manner similar to that described in Example 2-3, a transparent glass substrate that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer, was deposited by CVD to 0.4 microns. Then, an Al-Zr (97:3) alloy, serving as a G-S metal film layer for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film,

was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film not containing impurities and an amorphous silicon (n+a-Si) film containing an n-type impurity to 200 nm and 50 nm, respectively. Then, a first resist pattern for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Page 56, lines 8 to 24, cancel and replace with:

Thereafter, the n+a-Si film, the i-type a-Si film, the SiN_x film, and the Al-Zr film were sequentially etched, thereby forming a first pattern including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, and a semiconductor film, which were stacked, and a first comb-shaped pixel electrode 261.

Next, the gate electrode, the gate wiring line, and the first comb-shaped pixel electrode 261 were anodically oxidized in an electrolyte of ammonium borate to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a contact metal film layer (Ti) and a metal electrode film composed of an aluminum film (Al) were vapor deposited by

sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact electrode metal film and the metal electrode film were to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and were to connect together segments of each severed source segmented wiring line.

Page 56, line 25, to Page 57, line 19, cancel and replace with:

Subsequently, a second resist pattern for the second photolithography, which includes second comb-shaped pixel metal electrodes, was formed by a conventional method. Then, part of the metal electrode film, the contact metal film layer (Ti), and the n+a-Si film on the gate electrode were sequentially etched away, thus forming channel regions. The source segmented wiring line 209′ was connected to a source region by a portion of a contact metal film layer (Ti) and a metal electrode film pattern, and a second comb-shaped pixel metal electrode 262 was connected to a drain region by a portion of the contact electrode metal.

At this point, segments of the source segmented wiring line, which had been previously severed, were connected together on the

gate wiring line by the portion of the contact metal film layer (Ti) pattern and the metal electrode film pattern.

Finally, by using printing and baking a passivation film of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal which were to be connected to driving circuitry were etched away, thus producing a TFT array substrate 263 having the second comb-shaped pixel metal electrodes in the pixel portions (Figs. 23(a) and 23(b)).

Page 58, line 18, to Page 59, line 1, cancel and replace with:

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-7, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the second comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second electrodegroups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured,

and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Page 59, line 21, to Page 60, line 10, cancel and replace with:

In a manner similar to that described in Example 2-1, a transparent glass substrate that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer, was deposited by CVD to 0.4 microns. Then, an Al-Zr (97:3) alloy, serving as a G-S metal film layer for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film not containing impurities and an amorphous silicon (n+a-Si) film containing an n-type impurity to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern for the first photolithography was formed by a conventional method.

Page 60, lines 11 to 21, cancel and replace with:

Then, the Ti metal film, the n+a-Si film, the i-type a-Si film, the SiN_x film, and the Al-Zr film were sequentially etched, thereby forming a first pattern including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, a semiconductor film, and a contact electrode metal which were stacked.

Next, the gate electrode and the gate wiring line were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Page 61, lines 3 to 18, cancel and replace with:

Subsequently, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a conventional method. Then, part of the transparent conductive film, the contact electrode, and the n+a-Si film on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. The source segmented wiring line was connected to a source region by a

portion of the contact electrode metal and a metal electrode, and the first comb-shaped pixel metal electrode 271 was connected to a drain region by a portion of the contact electrode metal.

At this point, the source segmented wiring lines and, which had been previously severed, were connected together on the gate wiring line by the metal electrode via a portion of the contact electrode metal.

Subsequently, a silica passivation film of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film and the SiN_x film on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

Page 62, lines 15 to 20, cancel and replace with:

Furthermore, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact electrode metal film layer, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring

line, allowing fabrication of a TFT array substrate having few variations in characteristics.

Page 63, line 14, to Page 64, line 5, cancel and replace with:

First, there were provided a TFT array substrate, similar to that of Example 2-9, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the first comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates and were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns, which is created by spacers and adhesives. Thereafter, a TN liquid crystal was injected between the first and second substrates, and polarizers

and were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Page 64, line 16, to Page 65, line 3, cancel and replace with:

In a manner similar to that described in Example 2-8, a transparent glass substrate that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer, was deposited by CVD to 0.4 microns. Then, an Al-Zr (97:3) alloy, serving as a G-S metal film layer for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film not containing impurities and an amorphous silicon (n+a-Si) film containing an n-type impurity to 50 nm and 50 nm, respectively, and then a first resist pattern for the first photolithography was formed by a conventional method.

Page 65, lines 4 to 20, cancel and replace with:

Thereafter, the n+a-Si film, the i-type a-Si film, the SiN_x film, and the Al-Zr film were sequentially etched, thereby forming a first pattern including a gate electrode or a gate wiring line, a source segmented wiring line, a gate insulating film layer, and a semiconductor film which were stacked.

Next, the gate electrode and the gate wiring line were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a Ti metal film, serving as a contact metal film layer, was vapor deposited by sputtering to a film thickness of about 100 nm, and subsequently an Al-Zr film, serving as a metal electrode film, was vapor deposited by sputtering to a film thickness of about 100 nm. The contact metal film layer and the metal electrode film are to be connected to source regions and to first comb-shaped pixel metal electrodes connected to drain regions, and to connect together segments of each severed source segmented wiring line.

Page 65, line 21, to Page 66, line 4, cancel and replace with:

Thereafter, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a conventional method. Subsequently, part of the transparent conductive film, the contact metal film layer, and the n+a-Si film on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. The source segmented wiring line was connected to a source region by a portion of the contact electrode metal and a metal electrode, and the first comb-shaped pixel metal electrode 281 was connected to a drain region by a portion of the contact electrode metal.

Page 66, lines 5 to 19, cancel and replace with:

At this point, the source segmented wiring lines and, which had been previously severed, were connected together on the gate wiring line by the two-layered structure composed of the metal electrode and a portion of the contact electrode metal.

Subsequently, a silica passivation film of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a

mask, portions of the i-type a-Si film and the SiN_x film on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

Finally, an Al-Zr alloy was once again vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode 282 was formed, thus producing a TFT array substrate 283 applicable to IPS mode transmissive liquid crystal display devices, with the use of three photomasks (Figs. 25(a) and 25(b)).

Page 67, lines 6 to 21, cancel and replace with:

First, there were provided a TFT array substrate, similar to that of Example 2-11, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the first comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured,

and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates and were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns, which is created by spacers and adhesives. Thereafter, a TN liquid crystal was injected between the first and second substrates, and polarizers and were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Page 68, lines 1 to 6, cancel and replace with:

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

<u>IN THE CLAIMS</u>:

Please amend claims 15 to 18, 24, 46, 31, 36, 39, 41, 42, 44, 49, 57, 58, 60, 62 to 64, 67, 72, 75, 77, 78, 80, 85, 90, 93, 94, 96 and 98 to 101 as follows:

15. (Amended) A method of fabricating a bottom-gate TFT array substrate comprising:

(A) sequentially depositing at least a G-S metal film layer, a gate insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines;

(B), after step (A), by photolithography, using a first resist pattern, etching the layers through to the surface of the insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate

insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines;

(C), after step (B), oxidizing side surfaces of the gate electrodes and side surfaces of the gate wiring lines to form an electrically insulating metal oxide film;

(D), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and

(E), after step (D), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a predetermined pattern to form pixel electrodes and etching the contact metal film of the gate electrode section

pattern through to a surface of the semiconductor film to form channel regions on the semiconductor film.

16. (Amended) The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein the oxidation of the side surfaces of the gate electrodes and the side surfaces of the gate wiring lines is carried out by anodic oxidation.

17. (Amended) The method of fabricating a bottom-gate TFT array substrate according to claim 15 wherein:

the semiconductor film layer has a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and

step (E) of etching the contact metal film of the gate electrode section pattern is carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous silicon layer.

18. (Amended) The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein in place of the transparent conductive film layer in step (D), a light reflective conductive film layer is deposited.

24. (Amended) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the reflective pixel metal electrodes has a two-layered structure composed of a contact electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode.

26. (Amended) The bottom-gate TFT array substrate according to claim 24, wherein part of each source segmented wiring line has a two-layered structure composed of a contact metal film and an aluminum-based metal electrode film.

27. (Amended) The bottom-gate TFT array substrate according to claim 24, wherein the gate insulating film and the semiconductor film are formed between the gate electrode metal and the contact electrode metal.

28. (Amended) The bottom-gate TFT array substrate according to claim 24, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact electrode metal and the metal electrode.

31. (Amended) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor

film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact metal film and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact metal film, and the semiconductor film, using a second pattern.

36. (Amended) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact

electrode metal and a metal electrode; and

a color filter substrate having a color filter side on which a counter transparent electrode is formed;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

39. (Amended) A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact metal film and a metal

electrode film; and by photolithography, etching part of the metal electrode film, the contact metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the first substrate;

forming an alignment film on a surface of a counter electrode side of a second color filter substrate having a counter transparent electrode formed thereon;

adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

41. (Amended) The method of fabricating a liquid crystal display device according to claim 39, wherein the metal electrode and the contact electrode metal are formed in a single layer with a same material.

42. (Amended) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized;

each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

44. (Amended) The bottom-gate TFT array substrate according to claim 42, wherein the first comb-shaped pixel electrodes and part of each source segmented wiring line have a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact metal film layer, and a metal electrode film.

49. (Amended) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate;

by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes;

forming a metal electrode film; and

by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern.

57. (Amended) A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate

insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern;

forming an alignment film on the first substrate;

forming an alignment film on a surface of a second color filter substrate;

adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

58. (Amended) The method of fabricating a liquid crystal display device according to claim 57, further comprising:

after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film; and

using the passivation film as a mask, etching the metal electrode film, the contact metal film layer, the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

60. (Amended) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact electrode metal

and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode.

62. (Amended) The bottom-gate TFT array substrate according to claim 60, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact metal film layer, and a metal electrode film.

63. (Amended) The bottom-gate TFT array substrate according to claim 60, wherein the contact electrode metal is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

64. (Amended) The bottom-gate TFT array substrate according to claim 60, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact electrode metal and the metal electrode.

67. (Amended) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes;

forming a contact metal film layer and a metal electrode film; and

by photolithography, etching part of the metal electrode film,

the contact metal film layer, and the semiconductor film, using a second pattern.

72. (Amended) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact electrode metal and a metal electrode; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

75. (Amended) A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact metal film layer and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact metal film layer, and the semiconductor film,

using a second pattern;

forming an alignment film on the first substrate;

forming an alignment film on a surface of a counter electrode side of a second color filter substrate;

adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

77. (Amended) The method of fabricating a liquid crystal display device according to claim 75, wherein the metal electrode and the contact electrode metal are formed in a single layer with a same material.

78. (Amended) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped pixel electrodes are formed with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate.

80. (Amended) The bottom-gate TFT array substrate according to claim 78, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

85. (Amended) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate;

by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and

forming second comb-shaped pixel electrodes using a third pattern with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate.

90. (Amended) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped pixel electrodes formed with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

93. (Amended) A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate;

forming an alignment film on the first substrate;

forming an alignment film on a surface of a color filter side of a second color filter substrate;

adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

94. (Amended) The method of fabricating a liquid crystal display device according to claim 93, further comprising, after the formation of the second comb-shaped pixel electrodes, covering at least part of each second comb-shaped pixel electrode by a passivation film.

96. (Amended) A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and

another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped pixel electrodes are formed with a passivation film disposed between the second-comb shaped pixel electrodes and the substrate.

98. (Amended) A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact metal film layer and a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and

forming second comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate.

99. (Amended) A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped pixel electrodes formed with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate;

and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

100. (Amended) A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact metal film layer and a metal electrode film; by photolithography, sequentially etching part of the

metal electrode film, the contact metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped pixel electrodes and the substrate;

forming an alignment film on the first substrate;

forming an alignment film on a surface of a color filter side of a second color filter substrate;

adhering and fixing the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

101. (Amended) A method of fabricating a liquid crystal display device according to claim 100, further comprising covering at least part of each second comb-shaped pixel electrode by a passivation film.

Serial No. New Application

REMARKS

Claims 1-101, as amended, remain herein. Claims 15 to 18, 24, 46, 31, 36, 39, 41, 42, 44, 49, 57, 58, 60, 62 to 64, 67, 72, 75, 77, 78, 80, 85, 90, 93, 94, 96 and 98 to 101 have been amended hereby. Clarifying amendments have been made in the specification also.

Examination of this application on its merits is respectfully requested.

Respectfully submitted,

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ELECTRICAL CIRCUIT BOARD AND TFT ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME

TECHNICAL FIELD

The present invention relates to an innovative structure for electrical circuit boards having various applications, to TFT array substrates to which such electrical circuit boards are applied, and to liquid crystal display devices utilizing such TFT array substrates. The invention further relates to the fabrication methods of such electrical circuit boards, TFT array substrates, and liquid crystal display devices.

BACKGROUND ART

Conventionally, fabricating a TFT (Thin Film Transistor) array substrate for a color liquid crystal display device requires five to nine photomasks. As the number of photomasks to be used is increased, the number of the fabrication steps increases accordingly, and therefore the fabrication becomes complicated, making it difficult to reduce the fabrication cost.

Meanwhile, a technique for reducing the number of photomasks used in the fabrication process of a diode array substrate to two has been proposed (Published Japanese Translation of PCT International Publication for Patent Application No. 62-502361). However, the performance of diode array substrates is inferior to that of TFT (Thin Film Transistor) array substrates, and therefore the diode array substrate is not suitable for use in

color televisions.

DISCLOSURE OF THE INVENTION

In view of the foregoing, it is a principal object of the invention to provide an innovative structure that allows for reduction in the number of photomasks necessary for fabricating a TFT array substrate.

(1) A first aspect of the present invention (first to seventh embodiments) for achieving this object relates to a structure for electrical circuit boards applicable to semiconductor integrated circuits and the like. The first aspect of the present invention includes the following.

There is provided an electrical circuit board comprising; X wiring lines and Y segmented wiring lines, each of the wiring lines being formed of a same conductive metal film and in a same plane on an insulating substrate and the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines; wherein top and side surfaces of the X wiring lines are covered with an insulating film; and segments of each of the Y segmented wiring lines are electrically connected together by a Y segmented wiring line-connecting electrode formed on the insulating film.

With this construction, it is possible to build an X-Y wiring line intersection type electrical circuit, which allows an electric current to pass through independently, into an extremely thin plane, and therefore it is also possible to realize a multi-level integrated circuit. Hence, this construction is very compatible with semiconductor devices, and employing this construction allows remarkable increase in the degree of integration of

semiconductor circuits and the like.

In this construction, the insulating film of at least the side surfaces of the X wiring lines may be a metal oxide film formed by oxidizing the conductive metal film. In addition, the metal oxide film may be an anodic oxide film formed by anodic oxidation. The anodic oxide film is preferable because such a film is thin and provides excellent insulation.

The electrical circuit board having the above-described construction may be fabricated by the following fabrication method, with great productivity. Specifically, the method comprising: a first step of depositing a conductive metal film layer over an insulating substrate; a second step of etching the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines; a third step, after the second step, of oxidizing top and side surfaces of the X wiring lines to cover the top and side surfaces by an insulating metal oxide film; and a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

In this fabrication method, the third step of oxidizing the X wiring lines may be carried out by anodic oxidation. The anodic oxidation allows only the X wiring lines to be selectively and efficiently oxidized.

The electrical circuit board having the above-described construction

may also be fabricated by the following method, with great productivity. Specifically, the method comprising: a first step of sequentially depositing at least a conductive metal film layer and an insulating film layer over an insulating substrate; a second step of etching layers including the insulating film layer and the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines; a third step, after the second step, of oxidizing side surfaces of the X wiring lines to cover the side surfaces by an insulating metal oxide film; and a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

In this fabrication method also, the third step of oxidizing the side surfaces of the X wiring lines may be carried out by anodic oxidation.

(2) A second aspect of the present invention (eighth to eighteenth embodiments) relates to a bottom-gate TFT array substrate to which the above-described electrical circuit board is applied, and includes the following.

There is provided a bottom-gate TFT array substrate comprising: gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film; a gate insulating film

stacked on each of the gate electrodes; a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions; source contact electrodes stacked on the source regions of the semiconductor film; drain contact electrodes stacked on the drain regions of the semiconductor film; pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes; gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film; source segmented wiring lines formed in a same plane as the gate wiring lines, each of the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines.

With this construction, it is possible to provide a bottom-gate TFT array substrate with excellent reliability.

In this construction, the pixel electrodes and the source wiring line-connecting electrodes may be composed of a same transparent conductive film material.

Further, the substrate may be constructed such that a source segmented wiring line section pattern has a five-layered structure composed of the source segmented wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the source segmented wiring lines are located at the bottom of the five-layered

structure; a gate wiring line section pattern has a five-layered structure composed of the gate wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the gate wiring lines are located at the bottom of the five-layered structure; and the source segmented wiring lines and the gate wiring lines are in the same plane on the substrate.

In addition, the insulating film of at least the side surfaces of the gate wiring lines may be composed of an oxide film formed from the conductive metal film.

Moreover, the oxide film may be an anodic oxide film formed by anodic oxidation.

The substrate may also be constructed such that the semiconductor film has a two-layered structure composed of an i-type amorphous silicon layer and an n-type amorphous silicon layer.

Furthermore, in place of the transparent conductive film material, a light reflective conductive film material may be used. Thereby, it is possible to construct a bottom-gate TFT array substrate for reflective devices.

The above-described bottom-gate TFT array substrate may be fabricated by the following fabrication method, with great productivity.

Specifically, the method comprising: (A) sequentially depositing at least a G-S metal film layer, a gate insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines; (B), after step (A), by

photolithography, using a first resist pattern, etching the layers through to the surface of the insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines; (C), after step (B), ~~etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form on the semiconductor film, and~~ oxidizing side surfaces of the gate electrodes and side surfaces of the gate wiring lines to form an electrically insulating metal oxide film; ~~(E)~~ (D), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and ~~(F)~~ (E), after step ~~(E)~~ (D), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a predetermined pattern to form pixel

electrodes and ~~channel regions exposed by the etching~~ etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form channel regions on the semiconductor film.

In this fabrication method, the oxidation of the side surfaces of the gate electrodes and the side surfaces of the gate wiring lines may be carried out by anodic oxidation.

In addition, the semiconductor film layer may have a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and step ~~(F)~~(E) of etching the contact metal film of the gate electrode section pattern may be carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous silicon layer.

Furthermore, in place of the transparent conductive film layer in step ~~(E)~~(D), a light reflective conductive film layer may be deposited.

(3) A third aspect of the present invention (nineteenth to twenty-third embodiments) relates to a liquid crystal display device utilizing a bottom-gate TFT array substrate, and includes the following.

There is provided a liquid crystal display device comprising; a bottom-gate TFT array substrate including gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film; a gate insulating film stacked on the gate electrodes; a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel

regions between the source regions and the drain regions; source contact electrodes stacked on the source regions of the semiconductor film; drain contact electrodes stacked on the drain regions of the semiconductor film; pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes; gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film; source segmented wiring lines formed in a same plane as the gate wiring lines, the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines; and a counter substrate; wherein the TFT array substrate and the counter substrate are opposed to each other with a surface on which the TFTs are being formed facing inside and with a predetermined gap therebetween, a liquid crystal being held in the gap.

It is possible to further add the following to this construction. Specifically, the construction may be such that a surface of the TFT array substrate is protected by a passivation film. In addition, the passivation film may be one selected from the group consisting of a silica film and a silicon nitride film.

Furthermore, the pixel electrodes may be composed of a transparent metal film.

Moreover, the pixel electrodes may be composed of a light reflective metal film.

(4) A fourth aspect of the present invention (twenty-fourth to thirtieth embodiments) relates to a bottom-gate TFT array substrate, and includes the following.

(Twenty-fourth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the reflective pixel metal electrodes has a two-layered structure composed of a contact ~~metal~~ electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact ~~metal~~ electrode metal; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact ~~metal~~ electrode metal and a metal electrode.

(Twenty-fifth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the reflective pixel metal electrode group is one selected from the group consisting of aluminum and an aluminum-based alloy.

(Twenty-sixth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that part of each source segmented wiring line has a two-layered structure composed of a contact ~~electrode~~ metal film and an aluminum-based metal electrode film.

(Twenty-seventh embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the gate insulating film and the semiconductor film are formed between the gate electrode metal and the contact ~~metal~~ electrode metal.

(Twenty-eighth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact ~~metal~~ electrode metal and the metal electrode.

(Twenty-ninth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n+-type layer.

(Thirtieth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

(5) A fifth aspect of the present invention (thirty-first to thirty-fifth embodiments) includes the following.

(Thirty-first embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating

substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact ~~electrode~~ metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact ~~electrode~~ metal film, and the semiconductor film, using a second pattern.

(Thirty-second embodiment)

In the fabrication method according to the thirty-first embodiment, the metal electrode film may be an aluminum or aluminum-based alloy film.

(Thirty-third embodiment)

The fabrication method according to the thirty-first embodiment may further comprise forming a silica-based undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Thirty-fourth embodiment)

In the fabrication method according to the thirty-first embodiment, at least an aluminum-based alloy film may be formed for the gate wiring line metal film.

(Thirty-fifth embodiment)

In the fabrication method according to the thirty-first embodiment, the oxidation may be carried out, by anodic oxidation, in a neutral solution.

(6) A sixth aspect of the present invention (thirty-sixth to thirty-eighth embodiments) includes the following.

(Thirty-sixth embodiment)

There is provided a liquid crystal display device comprising: a

bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each having a two-layered structure composed of a contact ~~metal~~ electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact ~~metal~~ electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact ~~metal~~ electrode metal and a metal electrode; and a color filter substrate having a color filter side on which a counter transparent electrode is formed; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Thirty-seventh embodiment)

The liquid crystal display device according to the thirty-sixth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Thirty-eighth embodiment)

The liquid crystal display device according to the thirty-seventh embodiment may be such that the passivation film is an inorganic substance.

(7) A seventh aspect of the present invention (thirty-ninth to forty-first embodiments) includes the following.

(Thirty-ninth embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact ~~electrode~~ metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact ~~electrode~~ metal film, and the semiconductor film, using a second pattern; forming an alignment film on the ~~bottom-gate TFT array~~ first substrate; forming an alignment film on a surface of a counter electrode side of a second color filter substrate having a counter transparent electrode formed thereon; adhering and fixing the ~~bottom-gate TFT array substrate~~ first and second substrates and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Fortieth embodiment)

The fabrication method according to the thirty-ninth embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

(Forty-first embodiment)

The fabrication method according to the thirty-ninth embodiment may be such that the metal electrode and the contact ~~metal~~ electrode metal are formed in a single layer with a same material.

(8) An eighth aspect of the present invention (forty-second to forty-eighth embodiments) includes the following.

(Forty-second embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized; each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

(Forty-third embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the oxide film of the side surfaces of the gate electrodes and of the first comb-shaped pixel electrodes is an anodic oxide film.

(Forty-fourth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the first comb-shaped pixel electrodes and

part of each source segmented wiring line have a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact ~~electrode~~ metal film layer, and a metal electrode film.

(Forty-fifth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the contact electrode metal is formed to connect each of the comb-shaped electrodes to the semiconductor film.

(Forty-sixth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines and the first comb-shaped electrodes, and segments of each source segmented wiring line are interconnected together on the gate wiring lines and the first comb-shaped electrodes by a contact electrode metal and the metal electrode.

(Forty-seventh embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

(Forty-eighth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and a gate wiring line metal film.

(9) A ninth aspect of the present invention (forty-ninth to fifty-third embodiments) includes the following.

(Forty-ninth embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact ~~electrode~~ metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact ~~electrode~~ metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern.

(Fiftieth embodiment)

The fabrication method according to the forty-ninth embodiment may be such that portions to be formed into the gate wiring lines, the gate electrodes, and the first comb-shaped pixel electrodes are simultaneously etched.

(Fifty-first embodiment)

The fabrication method according to the forty-ninth embodiment may further comprise forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Fifty-second embodiment)

The fabrication method according to the forty-ninth embodiment may be such that at least the gate wiring line metal film, the gate insulating film,

and the semiconductor film are sequentially formed.

(Fifty-third embodiment)

The fabrication method according to the forty-ninth embodiment may be such that the oxidation is carried out by anodic oxidation.

(10) A tenth aspect of the present invention (fifty-fourth to fifty-sixth embodiments) includes the following.

(Fifty-fourth embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes, gate wiring lines, and first comb-shaped electrodes, at least side surfaces of the gate electrodes, of the gate wiring lines, and of the first comb-shaped electrodes being oxidized; second comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Fifty-fifth embodiment)

The liquid crystal display device according to the fifty-fourth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Fifty-sixth embodiment)

The liquid crystal display device according to the fifty-fifth embodiment may be such that the passivation film is an inorganic substance.

(11) An eleventh aspect of the present invention (fifty-seventh to fifty-ninth embodiments) includes the following.

(Fifty-seventh embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact ~~electrode~~ metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact ~~electrode~~ metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern; forming an alignment film on the first ~~bottom-gate TFT array~~ substrate; forming an alignment film on a surface of a second color filter substrate; adhering and fixing the ~~bottom-gate TFT array substrate and the color filter substrate~~ first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a

specified liquid crystal between the first and second substrates.

(Fifty-eighth embodiment)

The fabrication method according to the fifty-seventh embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film; and using the passivation film as a mask, etching the metal electrode film, the contact ~~electrode~~ metal film layer, the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

(Fifty-ninth embodiment)

The fabrication method according to the fifty-eighth embodiment may be such that the passivation film is a silica film or a silicon nitride film.

(12) A twelfth aspect of the present invention (sixtieth to sixty-sixth embodiments) includes the following.

(Sixtieth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact ~~metal~~ electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact ~~metal~~ electrode metal; and each of the source segmented wiring lines is connected to a source region of a

corresponding TFT by two layers of a contact ~~metal~~ electrode metal and a metal electrode.

(Sixty-first embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that an aluminum-based metal is used for the gate electrodes, and the insulating film of the side surfaces is an anodic oxide film.

(Sixty-second embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact ~~electrode~~ metal film layer, and a metal electrode film.

(Sixty-third embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that the contact ~~metal~~ electrode metal is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

(Sixty-fourth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact ~~metal~~ electrode metal and the metal electrode.

(Sixty-fifth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

(Sixty-sixth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

(13) A thirteenth aspect of the present invention (sixty-seventh to seventy-first embodiments) includes the following.

(Sixty-seventh embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact ~~electrode~~ metal film layer and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern.

(Sixty-eighth embodiment)

The fabrication method according to the sixty-seventh embodiment may be such that the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer

is etched through to the i-type layer.

(Sixty-ninth embodiment)

The fabrication method according to the sixty-seventh embodiment may further comprise forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Seventy embodiment)

The fabrication method according to the sixty-seventh embodiment may be such that at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

(Seventy-first embodiment)

The fabrication method according to the sixty-seventh embodiment may be such that the oxidation is carried out by anodic oxidation.

(14) A fourteenth aspect of the present invention (seventy-second to seventy-fourth embodiments) includes the following.

(Seventy-second embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a contact ~~metal~~ electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact ~~metal~~ electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact ~~metal~~ electrode metal and a metal electrode; and a color filter

substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Seventy-third embodiment)

The liquid crystal display device according to the seventy-second embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Seventy-fourth embodiment)

The liquid crystal display device according to the seventy-second embodiment may be such that the passivation film is an inorganic substance.

(15) A fifteenth aspect of the present invention (seventy-fifth to seventy-seventh embodiments) includes the following.

(Seventy-fifth embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped

electrodes; forming a contact ~~electrode~~ metal film layer and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern; forming an alignment film on the first ~~bottom-gate TFT array~~ substrate; forming an alignment film on a surface of a counter electrode side of a second color filter substrate; adhering and fixing the ~~bottom-gate TFT array substrate~~ first and second substrates and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Seventy-sixth embodiment)

The fabrication method according to the seventy-fifth embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

(Seventy-seventh embodiment)

The fabrication method according to the seventy-fifth embodiment may be such that the metal electrode and the contact ~~metal~~ electrode metal are formed in a single layer with a same material.

(16) A sixteenth aspect of the present invention (seventy-eighth to eighty-fourth embodiments) includes the following.

(Seventy-eighth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate

insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and the second comb-shaped ~~opposing electrodes~~ pixel electrodes are formed with ~~an insulating~~ a passivation film disposed between the second comb-shaped ~~opposing electrodes~~ pixel electrodes and the substrate.

(Seventy-ninth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the oxide film of the side surfaces of the gate electrodes is an anodic oxide film.

(Eightieth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate ~~wiring line metal~~ insulating film, a semiconductor film, a contact ~~electrode~~ metal film layer, and a metal electrode film.

(Eighty-first embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the contact electrode metal is formed between the semiconductor film and a source electrode and between the semiconductor film and a drain electrode.

(Eighty-second embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by a contact electrode metal and the metal electrode.

(Eighty-third embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

(Eighty-fourth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

(17) A seventeenth aspect of the present invention (eighty-fifth to eighty-ninth embodiments) includes the following.

(Eighty-fifth embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact ~~electrode~~ metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact ~~electrode~~ metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a

metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped ~~opposing~~ pixel electrodes using a third pattern with ~~an insulating~~ a passivation film disposed between the second comb-shaped ~~opposing~~ pixel electrodes and the substrate.

(Eighty-sixth embodiment)

The fabrication method according to the eighty-fifth embodiment may be such that the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched.

(Eighty-seventh embodiment)

The fabrication method according to the eighty-fifth embodiment may further comprise forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Eighty-eighth embodiment)

The fabrication method according to the eighty-fifth embodiment may be such that at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

(Eighty-ninth embodiment)

The fabrication method according to the eighty-fifth embodiment may be such that the oxidation is carried out by anodic oxidation.

(18) An eighteenth aspect of the present invention (ninetieth to ninety-second embodiments) includes the following.

(Embodiment ninetieth)

There is provided a liquid crystal display device comprising: a

bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped ~~opposing~~ pixel electrodes formed with ~~an insulating~~ a passivation film disposed between the second comb-shaped ~~opposing~~ pixel electrodes and the substrate; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Ninety-first embodiment)

The liquid crystal display device according to the ninetieth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Ninety-second embodiment)

The liquid crystal display device according to the ninety-first embodiment may be such that the passivation film is an inorganic substance.

(19) A nineteenth aspect of the present invention (ninety-third to ninety-fifth embodiments) includes the following.

(Ninety-third embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact ~~electrode~~ metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact ~~electrode~~ metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped ~~opposing~~ pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped ~~opposing~~ pixel electrodes and the substrate; forming an alignment film on the ~~bottom-gate TFT array~~ first substrate; forming an alignment film on a surface of a color filter side of a second color filter substrate; adhering and fixing the ~~bottom-gate TFT array substrate and the color filter substrate~~ the first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Ninety-fourth embodiment)

The fabrication method according to the ninety-third embodiment may

further comprise, after the formation of the second comb-shaped ~~opposing~~ pixel electrodes, covering at least part of each second comb-shaped ~~opposing~~ pixel electrode by a passivation film.

(Ninety-fifth embodiment)

The fabrication method according to the ninety-third embodiment may be such that the passivation film is a silica film or a silicon nitride film.

(20) A twentieth aspect of the present invention (ninety-sixth and ninety-seventh embodiments) includes the following.

(Ninety-sixth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal; each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and the second comb-shaped ~~opposing~~ pixel electrodes are formed with ~~an insulating~~ a passivation film disposed between the second-comb shaped ~~opposing~~ pixel electrodes and the substrate.

(Ninety-seventh embodiment)

The bottom-gate TFT array substrate according to the ninety-sixth

embodiment may be such that at least segments of each source segmented wiring line are connected together by a two-layered structure composed of the metal electrode and a contact electrode metal.

(21) A twenty-first aspect of the present invention (ninety-eighth embodiment) includes the following.

(Ninety-eighth embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact ~~electrode~~ metal ~~film~~ layer and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact ~~electrode~~ metal ~~film~~ layer, and the semiconductor film, using a second pattern; and forming second comb-shaped ~~opposing~~ pixel electrodes, using a third pattern, with ~~an insulating~~ a passivation film disposed between the second comb-shaped ~~opposing~~ pixel electrodes and the substrate.

(22) A twenty-second aspect of the present invention (ninety-ninth embodiment) includes the following.

(Ninety-ninth embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the

gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped ~~opposing~~ pixel electrodes formed with ~~an insulating~~ a passivation film disposed between the second comb-shaped ~~opposing~~ pixel electrodes and the substrate; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(23) A twenty-third aspect of the present invention (hundredth and hundred-first embodiments) includes the following.

(Hundredth embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact ~~electrode~~ metal film

layer and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact ~~electrode~~ metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped ~~opposing~~ pixel electrodes, using a third pattern, with ~~an insulating~~ a passivation film disposed between the second comb-shaped ~~opposing~~ pixel electrodes and the substrate; forming an alignment film on the ~~bottom-gate TFT array~~ first substrate; forming an alignment film on a surface of a color filter side of a second color filter substrate; adhering and fixing the ~~bottom-gate TFT array substrate and the color filter substrate~~ first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Hundred-first embodiment)

The fabrication method may further comprise covering at least part of each second comb-shaped ~~opposing~~ pixel electrode by a passivation film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view illustrating a process step for fabricating an electrical circuit board in accordance with Example 1-1 of the present invention.

Fig. 2 is a plan view showing the state of the substrate surface that has been etched using a first resist pattern in accordance with Example 1-1 of the present invention.

Fig. 3 is a plan view showing the state where a conductive film layer is

deposited on the entire surface of the substrate in accordance with Example 1-1 of the present invention.

Fig. 4 is a plan view showing the state where the conductive film layer on the substrate has been processed into a predetermined pattern (Y segmented wiring line-connecting electrodes) in accordance with Example 1-1 of the present invention.

Figs. 5(a) and 5(b) are schematic cross-sectional views illustrating a process step for fabricating a TFT array in accordance with Example 2-1 of the present invention.

Figs. 6(a) and 6(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Fig. 7 is a schematic top plan view of Fig. 6(b).

Figs. 8(a) and 8(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Figs. 9(a) and 9(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Figs. 10(a) and 10(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Figs. 11(a) and 11(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Fig. 12 is a schematic plan view of the TFT array substrate in accordance with Example 2-1.

Fig. 13 is a schematic cross-sectional view illustrating a liquid crystal display device in accordance with Example 2-2 of the present invention.

Figs. 14(a) and 14(b) are views illustrating a process step for fabricating a TFT array in accordance with Example 2-3 of the present invention.

Figs. 15(a) and 15(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 16(a) and 16(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 17(a) and 17(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 18(a) and 18(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 19(a) and 19(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 20(a) and 20(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Fig. 21 is a schematic cross-sectional view illustrating a liquid crystal display device in accordance with Example 2-4 of the present invention.

Figs. 22(a) and 22(b) are schematic cross-sectional views of a TFT in accordance with Example 2-5 of the present invention.

Figs. 23(a) and 23(b) are schematic cross-sectional views of a TFT in accordance with Example 2-7 of the present invention.

Figs. 24(a) and 24(b) are schematic cross-sectional views of a TFT in accordance with Example 2-9 of the present invention.

Figs. 25(a) and 25(b) are schematic cross-sectional views of a TFT in accordance with Example 2-11 of the present invention.

Fig. 26 is a view showing the entire TFT array substrate in accordance with Example 2-1 of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention is described in more detail below with reference to examples thereof.

Example 1-1

A transparent glass substrate (insulating substrate) 101 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film layer, serving as an undercoat film layer 102, was deposited by CVD to a thickness of 0.4 microns. Subsequently, an Al–Zr (97:3) alloy film layer, serving as a metal film layer 103 for forming X wiring lines and Y segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Further, a SiN_X film, serving as an insulating film layer 104, was deposited by plasma enhanced CVD to 150 nm (Fig. 1).

Next, by photolithography using a first resist pattern 105 (Fig. 1), the layers were etched from the top of the insulating film layer 104 through to the undercoat film layer 102, to form X wiring lines 106 and Y segmented wiring lines 107 in a pattern on the substrate, the Y segmented wiring lines being severed by the X wiring lines at the intersections of the X wiring lines and the Y segmented wiring lines and being spaced apart from the X wiring lines (Fig. 2).

Then, by immersing the entire substrate in an electrolyte using ammonium borate and having a pH of about 7 and passing an electric current only through the X wiring lines from the periphery of the substrate (anodic oxidation), the side surfaces of the X wiring lines were oxidized, thus forming insulating metal oxide films 106' (mainly composed of Al_2O_3) on the side surfaces of the X wiring lines.

Subsequently, a conductive film layer 108 composed of, for example, indium tin oxide (ITO) was deposited on top of the insulating film layer 104 over the entire surface of the substrate so as to fill the space between the X wiring lines and the Y segmented wiring lines (Fig. 3). Thereafter, unwanted areas of the conductive film on the insulating film were etched using a second resist pattern, as is shown in Fig. 4, to form Y segmented wiring line-connecting electrodes 109. As a result of this etching, electrical conduction between adjacent Y segmented wiring lines arranged parallel to one another is prevented and electrical conduction (connection) between segments of each Y segmented wiring line severed by the X wiring lines at the intersections of the X wiring lines and the Y segmented wiring lines is able to be realized by the Y segmented wiring line-connecting electrode 109,

thus completing an electrical circuit board in accordance with Example 1-1 having such a structure.

Example 1-2

In Example 1-2, an insulating film layer 104 was not deposited. By using the above-described first resist pattern 105, a metal film layer 103 was etched to an undercoat film layer 102, thus forming X wiring lines and Y segmented wiring lines with no insulating films stacked thereon.

Subsequently, in a manner similar to that described in foregoing Example 1-1, the X wiring lines were oxidized by anodic oxidation to cover the side surfaces and top surfaces thereof by oxide films, mainly composed of Al_2O_3. It should be noted that in Example 1-2 both the top and side surfaces of the X wiring lines were oxidized in a manner similar to that described in the foregoing Example 1-1 because the metal film layer 103 was not covered by the insulating film layer 104 as was the case with Example 1-1.

Next, a conductive film layer (for example, ITO, Al, or the like) was deposited on the entire surface of the substrate, and then using a second resist pattern, unwanted areas of the conductive film layer were etched away in a manner similar to that described in Example 1-1. Thereby, an electrical circuit board in accordance with Example 1-2 was completed in which there is no connection between adjacent Y segmented wiring lines arranged parallel to one another and in which segments of each Y segmented wiring line severed at the intersections of the X wiring lines and the Y segmented wiring lines are connected together by the conductive film.

It should be noted that in Examples 1-1 and 1-2 the surface of the metal film was oxidized by anodic oxidation because this method allows insulating films, formed from the metal oxide film, to be selectively formed only on the X wiring lines, providing superior productivity.

It should also be understood that in the foregoing Fig. 4, the connecting electrodes were formed in a belt shape lying along the Y segmented wiring lines, but the shape is not limited thereto. For example, the shape of the second resist pattern may be changed so as to form a square- or circle-shaped connecting electrode pattern that covers only the intersections of the X wiring lines and the Y segmented wiring lines.

<u>Example 2-1</u>

A transparent glass substrate (insulating substrate) 201 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to a thickness of 0.4 microns. Subsequently, an Al–Zr (97:3) alloy film, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Thereafter, a SiN_X film, serving as a gate insulating film layer 204, was deposited by plasma enhanced CVD to 150 nm. Then, as a semiconductor film layer 299, an amorphous silicon (i-type a-Si) film 205 not containing impurities and an amorphous silicon (n+a-Si) film 206 containing an n-type impurity were sequentially deposited to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer 207, was vapor deposited by sputtering to a film thickness

of about 100 nm, and a first resist pattern 208 for the first photolithography was then formed by a conventional method (Figs. 5(a) and 5(b)).

Thereafter, the contact metal film layer 207 (Ti metal film), the n+a-Si film layer 206, the i-type a-Si film layer 205, the gate insulating film layer 204 (SiN_X film), and the G-S metal film layer 203 (Al–Zr film) were sequentially etched, thereby forming a first pattern 210 including a gate electrode 203' or a gate wiring line 203", source segmented wiring lines 209' and 209", a gate insulating film 204', the semiconductor film 299 (205' and 206'), and a contact metal film 207' which were stacked (Figs. 6(a) and 6(b)).

A schematic top plan view of Fig. 6(b) is shown in Fig. 7. As can be seen from Fig. 7, the gate wiring line 203" extends from the front to the end as viewed in the figure, and the source segmented wiring lines 209' and 209" extend in the direction orthogonal to the 203" (the horizontal direction as viewed in the figure). The source segmented wiring lines 209' and 209" are disconnected by the gate wiring line 203" crossing therebetween, and the gate wiring line 203" is spaced apart from each of the source segmented wiring lines 209' and 209" by a predetermined distance. It is preferable that the distance of the space be made approximately equal to the total thickness of all the layers (etching depth).

It should be noted that Fig. 6(b) is a cross-sectional view taken along the line X–Y of Fig. 7.

Next, the gate electrode 203' and the gate wiring line 203" were selectively anodically oxidized in an electrolyte using ammonium borate and having a pH of about 7, to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the pattern (Figs. 8(a) and 8(b)).

Thereafter, a transparent conductive film 212, composed of an indium tin oxide (ITO) film, was vapor deposited by sputtering on the entire surface of the substrate to a film thickness of about 100 nm (Figs. 9(a) and 9(b)). The transparent conductive film 212 is to be connected to source regions and to pixel transparent electrodes 215, which are connected to drain regions, and also to connect together segments of each disconnected source segmented wiring line (i.e., serving as a source segmented wiring line-connecting electrode).

Subsequently, a second resist pattern 208' for the second photolithography (Figs. 10(a) and 10(b)) was formed by a conventional method. Then, part of the transparent conductive film 212, the contact metal film 207', and the n+a-Si film 206' on the gate electrode were sequentially etched away through to the i-type a-Si film 205', thus forming channel regions. ~~and the~~ The source segmented wiring line 209' was connected to a source region 213 by a portion of the contact electrode 207' and a transparent conductive film 214, and the pixel transparent electrode 215 was connected to a drain region 216 by a portion of the contact electrode 207' (Figs. 11(a) and 11(b)).

Thus, the disconnected source segmented wiring lines 209' and 209" are connected together by a transparent conductive film 214' and a portion of the contact metal film 207' on the gate wiring line 203" (Figs. 11(a) and 11(b)).

Finally, by using printing and baking a silica passivation film layer 217 of 300 nm was formed on the substrate, except for the periphery thereof, so as to cover the TFTs. Thereafter, using this silica passivation film pattern

as a mask, the peripheral portion of the stacked layers of the i-type a-Si film 205 and the gate insulating film layer 204 (SiN_x film), which is to be connected to external driving circuitry, was etched away to expose the gate G-S metal film 203 (see Fig. ~~26~~ 11). Thereby, a TFT array substrate 218 (Fig. 26) applicable to transmissive liquid crystal display devices was produced.

Fig. 12 is an enlarged schematic plan view of a main portion of the TFT array substrate 218 produced in the present example. Fig. 11(a) is a cross-sectional view taken along the line A–A' of Fig. 12, and Fig. 11(b) is a cross-sectional view taken along the line B–B' of Fig. ~~18~~ 12.

According to the present example described above, the gate wiring lines and the source segmented wiring lines are formed simultaneously in the same plane, and the side surfaces of the gate wiring lines are selectively oxidized by anodic oxidation for insulation. Segments of each source segmented wiring line, which has been disconnected by the gate wiring lines, are connected together by the contact metal film and the transparent conductive film that are stacked on each gate wiring line. Hence, the resistance of the source segmented wiring line is unlikely to increase substantially. In addition, with this structure, level differences on the surface of the TFT array can be sufficiently minimized.

Further, in fabricating a TFT array substrate, conventional methods required five to seven photomasks; on the other hand, the fabrication method of the present example requires only two photomasks. Therefore, according to the method of the present example, it is possible to significantly reduce the fabrication costs of a TFT array substrate.

Moreover, for stacking layers on the substrate, by sequentially depositing the G-S metal film layer, the gate insulating film layer, and the semiconductor film layer, it is possible to fabricate a highly reliable bottom-gate TFT array substrate with little contamination at the interfaces of the channel portions.

For oxidation, by carrying out anodic oxidation using an electrolyte with a pH of 7, it is possible to efficiently and selectively oxidize only the side surfaces of the gate electrodes and the side surfaces of the gate wiring lines connected to the gate electrodes. In addition, this method allows for formation of high quality oxide films with no pinholes, thus achieving wiring lines with little gate leakage.

In this example, the source segmented wiring lines have a five-layered structure composed of the G-S metal film, a gate insulating film, the semiconductor film, the contact metal film, and the conductive film, and therefore the overall resistance of the source segmented wiring lines is reduced.

In addition, in this example, the gate insulting film and the semiconductor film are deposited between the G-S metal film (the gate electrodes, gate wiring lines, and source segmented wiring lines) and the contact metal film (contact electrodes), and therefore current leakage is less likely to occur.

Furthermore, in this example, the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, whereby the contact resistance of the source and the drain can be reduced.

Since the undercoat film layer is disposed between the surface of the

insulating substrate and the gate wiring line metal film, diffusion of impurities from the substrate can be prevented.

In the present example, a TFT array substrate for a transmissive device was produced; but it is also possible to produce a TFT array substrate for a reflective device, i.e., applicable to reflective liquid crystal display devices, by using a high-reflective metal film such as Al or an Al alloy in place of the transparent conductive film.

Example 2-2

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-1 is described with reference to Fig. 13.

First, there were provided a TFT array substrate, similar to that of Example 2-1, fabricated using two masks, more specifically, a first TFT array substrate 223 including a first electrode group 221 arranged in a matrix and a transistor group 222 that drives the first electrodes; and a second color filter substrate 226 including a second electrode 225 and a color filter group 224 placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 227.

Next, the first and second substrates 223 and 226 were arranged such that their respective electrodes oppose one another, thus producing a cell having an alignment direction twisted 90 degrees and a gap of about 5 microns, created by spacers 228 and adhesives 229. Thereafter, a TN liquid

crystal 230 was injected between the first and second substrates, and polarizers 231 and 232 were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images in the direction of the arrow A, by driving each transistor using video signals while lighting the entire display using a backlight 233. Here, after the step of fabricating the bottom-gate TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array by a passivation film, it was possible to fabricate a liquid crystal display device with high reliability.

In addition, for the passivation film, using a silica film or a silicon nitride film, which is an inorganic substance, made it possible to fabricate a liquid crystal display device with even higher reliability.

Furthermore, by using such a TFT array substrate as to have a metal electrode film formed in place of the transparent conductive film, it was possible to fabricate a reflective liquid crystal display device.

<u>Example 2-3</u>

In a manner similar to that described in Example 2-1, a transparent glass substrate 201 that had been thoroughly cleaned was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy film, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate

insulating film layer 204, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film layer 205 not containing impurities and an amorphous silicon (n+a-Si) film layer 206 containing an n-type impurity to 200 nm and 50 nm, respectively.

It should be noted that in this example a contact metal film is not deposited on the n+a-Si film layer 206, which is different from the foregoing Example 2-1.

Next, a first resist pattern 208 for the first photolithography was formed by a conventional method (Figs. 14(a) and 14(b)).

Thereafter, the n+a-Si film layer 206, the i-type a-Si film layer 205, the gate insulating film layer 204 (SiN_x film), and the G-S metal film layer 203 (Al-~~Ta~~Zr film) were sequentially etched, thereby forming a first pattern 240 including a gate electrode 203' or a gate wiring line 203", a source segmented wiring line 209', a gate insulating film 204', and a semiconductor film (205'+206') which were stacked (Figs. 15(a) and 15(b)).

Then, the gate electrode 203' and the gate wiring line 203" were anodically oxidized in an electrolyte to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the gate electrode and the side surfaces of the gate wiring line (Figs. 16(a) and 16(b)). Thereafter, a contact ~~electrode~~ metal film (Ti) 241 and a metal electrode film 242 composed of an aluminum film (Al) were vapor deposited by sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact ~~electrode~~ metal film and the metal electrode film were to be connected to pixel metal electrodes connected to drain regions and were to connect

together segments of each severed source segmented wiring line connected to source regions (Figs. 17(a) and 17(b)).

Subsequently, a second resist pattern 208' for the second photolithography was formed by a conventional method (Figs. 18(a) and 18(b)). Then, part of the metal electrode film 242, the contact ~~electrode~~ metal film (Ti) 241, and the n+a-Si film 206' on the gate electrode were sequentially etched away, thus forming channel regions. ~~and the~~ The source segmented wiring line 209' was connected to a source region 213 by a portion of a contact ~~electrode~~ metal film (Ti) 241' and a metal electrode film pattern 242', and a pixel metal electrode film 243 was connected to a drain region 216 by the contact electrode metal 241' (Figs. 19(a) and 19(b)). At this point, segments of the source segmented wiring line 209', which had been previously severed and disconnected, were connected together on the gate wiring line 203" by the portion of the contact ~~electrode~~ metal film (Ti) 241' and the metal electrode film pattern 242' (Fig. 19(b)).

Finally, by using printing and baking a silica passivation film 217 of 300 nm was formed on the substrate, except for the periphery thereof, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal, which are to be connected to driving circuitry, were etched away, thus producing a TFT array substrate 245 having reflective pixel metal electrodes in the pixel portions (Figs. 20(a) and 20(b)).

According to the present example, segments of each source segmented wiring line are connected together by the two layers of the contact ~~metal~~ electrode metal and the metal electrode, and therefore the resistance of the

source segmented wiring lines was made extremely low.

In addition, by using aluminum or an aluminum-based alloy (such as an Al–Zr or Ag–Pd–Cu alloy) for the reflective pixel metal electrode, it was possible to fabricate a TFT array substrate with excellent reflectivity.

Moreover, by vapor depositing the silica-based undercoat film between the surface of the insulating substrate and the gate wiring line metal film by a sol-gel method, it was possible to absorb substrate deformation.

Forming the aluminum-based alloy film for the gate wiring line metal film made it possible to fabricate a TFT array substrate having few irregularities on the surface of the wiring lines.

In the step of oxidation, by carrying out anodic oxidation in a neutral solution, it was possible to fabricate a TFT array substrate having good gate insulating properties.

Here, when the oxide films of the side surfaces of the gate electrodes were neutral, anodic oxide films, it was possible to fabricate a TFT array substrate with high reliability.

In addition, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact ~~electrode~~ metal film, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring lines.

Forming the silicon nitride-based gate insulating film and the semiconductor film between the gate electrode metal and the contact ~~metal~~ electrode metal made it possible to fabricate a TFT array substrate having excellent stability.

When segments of each source segmented wiring line, which had been severed by the gate wiring lines, were interconnected together on the gate wiring lines by the two layers of the contact ~~metal~~ electrode metal and the metal electrode, it was possible to minimize level differences on the surface of the TFT array substrate.

Further, when part of the semiconductor film had a two-layered structure composed of an i-type layer and an n+-type layer, it was possible to reduce the contact resistance of the source and the drain.

Furthermore, when the undercoat film was formed between the surface of the insulating substrate and the gate wiring line metal film, it was possible to fabricate a TFT array substrate with high reliability.

Example 2-4

The actual fabrication process of a liquid crystal display device using the TFT array substrate obtained in Example 2-3 is described with reference to Fig. 21.

First, there were provided a TFT array substrate, similar to that of Example 2-3, fabricated using two masks, more specifically, a first TFT array substrate 323 including a first electrode group 321 arranged in a matrix and a transistor group 322 that drives the first electrodes; and a second color filter substrate 326 including a second electrode 325 and a color filter group 324 placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 327.

Next, the first and second substrates 323 and 326 were arranged such that their respective electrodes oppose one another, thus producing a cell having a gap of about 5 microns created by spacers 328 and adhesives 329. A TN liquid crystal 330 was then injected between the first and second substrates, and a polarizer 331 was arranged on the cell surface of the color filter side, thus completing a reflective liquid crystal display device.

Such a device was capable of displaying images in the direction of the arrow A, by driving each transistor using video signals.

<u>Example 2-5</u>

In a manner similar to that described in Example 2-1, a transparent glass substrate ~~201~~ that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer ~~202~~, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer ~~203~~ for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer ~~204~~, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film layer ~~205~~ not containing impurities and an amorphous silicon (n+a-Si) film layer ~~206~~ containing an n-type impurity to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer ~~207~~, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional

method.

Then, the ~~Ti metal film 207~~ contact metal film layer (Ti), the n+a-Si film layer ~~206~~, the i-type a-Si film layer ~~205~~, the gate insulating film layer (SiN_x film) ~~204~~, and the G-S metal film layer (Al–Zr film) ~~203~~ were sequentially etched, thereby forming a first pattern including a gate electrode ~~203'~~ or a gate wiring line ~~203''~~, a source segmented wiring line ~~209'~~, a gate insulating film layer ~~204'~~, and a semiconductor film ~~(205')~~, which were stacked, and a first comb-shaped pixel metal electrode 251.

Next, the gate electrode ~~203'~~, the gate wiring line ~~203''~~, and the first comb-shaped pixel metal electrode 251 were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films ~~211~~, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a metal (Al) electrode film was vapor deposited by sputtering to a film thickness of about 100 nm. The metal electrode film was to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and was to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography was formed by a conventional method. Then, part of the metal electrode film ~~212'~~, the contact electrode metal ~~207'~~, and the n+a-Si film 206' on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. ~~and the~~ The source segmented wiring line 209' was connected to a source region ~~213~~ by a portion of the contact electrode ~~7~~metal and a metal electrode ~~214'~~, and a second comb-shaped pixel

metal electrode ~~252~~ was connected to a drain region ~~216~~ by a portion of the contact electrode metal ~~207~~.

At this point, the source segmented wiring lines ~~209'~~ and ~~209''~~, which had been previously severed, were connected together on the gate wiring line ~~203~~ by the metal electrode film pattern ~~214~~ via a portion of the contact electrode metal ~~7~~.

Finally, by using printing and baking a silica passivation film 217 of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the i-type a-Si film ~~205~~ and the SiN_x film ~~204~~ on the gate electrode metal, which are to be connected to external driving circuitry, were etched away, thus producing a TFT array substrate 253 applicable to in-plane switching (IPS) mode liquid crystal display devices (Figs. 22(a) and 22(b)).

Here, by simultaneously etching portions that are to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes, it was possible to fabricate a TFT array substrate for the IPS mode device, without additional masks.

In addition, carrying out the step of forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to fabricate a TFT array substrate having excellent stability.

Moreover, by sequentially forming the gate wiring line metal film, the gate insulating film, and the semiconductor film, it was possible to prevent contamination of the channel portions.

In the oxidation step, carrying out anodic oxidation in a neutral

electrolyte made it possible to selectively oxidize and insulate only the side surfaces of the gate electrodes, the side surfaces of the gate wiring lines, and the side surfaces of the first comb-shaped pixel electrodes.

When the first comb-shaped pixel electrodes and part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact ~~electrode~~ metal film layer, and the metal electrode film, it was possible to provide a TFT array substrate having little resistance of the source segmented wiring line.

Further, when the contact electrode metal was formed for connecting the semiconductor films and the comb-shaped electrodes, it was possible to provide a TFT array substrate having low drain contact resistance.

When segments of each source segmented wiring line, which had been severed by the gate wiring lines and the first comb-shaped electrodes, were interconnected together on the gate wiring lines and the first comb-shaped electrodes by the contact electrode metal and the metal electrode, it was possible to provide a TFT array substrate having few level differences on the surface.

Moreover, when part of the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer, it was possible to provide a TFT array substrate having even lower contact resistance.

By forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film, it was possible to prevent impurities migrating from the substrate from diffusing, providing a TFT array substrate with high reliability.

Example 2-6

The actual fabrication process of an IPS mode liquid crystal display device using the above-described TFT array substrate is described.

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-5, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the ~~first electrodes~~ second comb shaped electrode group; and a color filter substrate including a second color filter substrate group placed opposite to the first and second electrode ~~group~~grouos. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns created by spacers and adhesives. Thereafter, a nematic liquid crystal was injected between the first and second substrates, and polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device. ~~(Drawings of the present example are similar to those in Figs. 19(a) and 19(b) except that a second electrode 225 is absent in the present example, and thus are omitted.)~~

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160°

horizontally and vertically with a contrast of 10.

At this point, after the step of fabricating TFT array substrate for the IPS mode device prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film, it was possible to fabricate a liquid crystal display device with high reliability.

Here, after the step of fabricating the bottom-gate TFT array substrate prior to the formation of the alignment films, by covering at least part of the TFT array substrate by a passivation film and etching, with use of this passivation film as a mask, the metal electrode film, the contact electrode metal film, the semiconductor film, and the gate insulating film to expose gate wiring line terminals, it was possible to fabricate a liquid crystal display device at low cost.

In addition, for the passivation film, forming a film composed of an inorganic substance such as a silica film or a silicon nitride film made it possible to fabricate a liquid crystal display device with excellent reliability.

<u>Example 2-7</u>

In a manner similar to that described in Example 2-3, a transparent glass substrate ~~201~~ that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer ~~202~~, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer ~~203~~ for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film ~~4~~, serving as a gate

insulating film, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film ~~205~~ not containing impurities and an amorphous silicon (n+a-Si) film ~~206~~ containing an n-type impurity to 200 nm and 50 nm, respectively. Then, a first resist pattern ~~208~~ for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Thereafter, the n+a-Si film~~-206~~, the i-type a-Si film~~-205~~, the SiN_x film ~~204~~, and the Al-~~Ta~~Zr film ~~203~~ were sequentially etched, thereby forming a first pattern including a gate electrode ~~203'~~ or a gate wiring line~~-203"~~, a source segmented wiring line~~-209'~~, a gate insulating film layer~~-204'~~, and a semiconductor film~~-(205')~~, which were stacked, and a first comb-shaped pixel electrode 261.

Next, the gate electrode~~-203'~~, the gate wiring line~~-203"~~, and the first comb-shaped pixel electrode 261 were anodically oxidized in an electrolyte of ammonium borate to form insulating films~~-211~~, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a contact ~~electrode~~ metal film layer (Ti)~~-film 241~~ and a metal electrode film ~~242~~ composed of an aluminum film (Al) were vapor deposited by sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact electrode metal film and the metal electrode film were to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and were to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography, which includes second comb-shaped pixel metal electrodes, was formed by a

conventional method. Then, part of the metal electrode film ~~242~~, the contact ~~electrode~~ metal film layer (Ti) ~~41~~, and the n+a-Si film ~~206'~~ on the gate electrode were sequentially etched away, thus forming channel regions ~~and the~~ The source segmented wiring line 209' was connected to a source region ~~213~~ by a portion of a contact ~~electrode~~ metal film layer (Ti) ~~film 241'~~ and a metal electrode film pattern ~~242'~~, and a second comb-shaped pixel metal electrode 262 was connected to a drain region ~~216~~ by a portion of the contact ~~metal~~ electrode metal.

At this point, segments of the source segmented wiring line ~~209'~~, which had been previously severed, were connected together on the gate wiring line ~~203'~~ by the portion of the contact ~~electrode~~ metal film layer (Ti) ~~film~~ pattern ~~241'~~ and the metal electrode film pattern ~~242'~~.

Finally, by using printing and baking a passivation film ~~217~~ of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal which were to be connected to driving circuitry were etched away, thus producing a TFT array substrate 263 having the second comb-shaped pixel metal electrodes in the pixel portions (Figs. 23(a) and 23(b)).

Here, when the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer and part of the n-type layer was etched to the i-type layer, it was possible to fabricate a TFT array substrate at low cost without additional masks.

Further, by forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film, it was possible to

prevent impurities generating from the substrate from diffusing, allowing fabrication of a TFT array substrate with high reliability.

When the gate wiring line metal film, the gate insulating film, and the semiconductor film were sequentially formed, contamination of the channel portions was kept to a minimum, allowing fabrication of a TFT array substrate having stable Vt.

In the step of oxidation, by carrying out anodic oxidation in a neutral solution, it was possible to fabricate a TFT array substrate having few pinholes and little leakage current.

Moreover, when part of the TFT array substrate was covered, using a sol-gel method, by a passivation film composed of silica or a silica-containing inorganic substance, it was possible to fabricate a TFT array substrate with high reliability.

Example 2-8

The actual fabrication process of a liquid crystal display device using the above-described TFT array substrate is described.

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-7, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group and a second comb-shaped electrode group arranged in a matrix and a transistor group that drives the ~~first electrodes~~ second comb-shaped electrode group; and a second color filter substrate including a color filter group placed opposite to the first and second electrode ~~group~~groups. Over each of the substrates, by a conventional method, a

polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 4 microns created by spacers and adhesives. In addition, a nematic liquid crystal was injected between the first and second substrates, and two polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

Furthermore, when the metal electrode and the contact metal electrode were formed in a single layer with the same material, it was possible to further simplify the process.

<u>Example 2-9</u>

In a manner similar to that described in Example 2-1, a transparent glass substrate ~~1~~ that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer ~~202~~, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a

G-S metal film layer ~~203~~ for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer ~~204~~, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film ~~205~~ not containing impurities and an amorphous silicon (n+a-Si) film ~~206~~ containing an n-type impurity to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer ~~207~~, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern ~~208~~ for the first photolithography was formed by a conventional method.

Then, the Ti metal film ~~207~~, the n+a-Si film ~~206~~, the i-type a-Si film ~~205~~, the SiN_x film ~~204~~, and the Al–Zr film ~~203~~ were sequentially etched, thereby forming a first pattern ~~210~~ including a gate electrode ~~202'~~ or a gate wiring line ~~202"~~, a source segmented wiring line ~~209'~~, a gate insulating film layer ~~204'~~, a semiconductor film ~~(205' and 206')~~, and a contact electrode metal ~~207'~~ which were stacked.

Next, the gate electrode ~~2'~~ and the gate wiring line ~~2"~~ were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films ~~211~~, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a metal electrode film was vapor deposited by sputtering to a film thickness of about 100 nm. The metal electrode film was to be connected to source regions and to first comb-shaped pixel metal electrodes connected to drain regions and was to connect together segments of each

severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a conventional method. Then, part of the transparent conductive film ~~212~~, the contact electrode ~~207'~~, and the n+a-Si film ~~206'~~ on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. ~~and the~~ The source segmented wiring line ~~209'~~ was connected to a source region ~~213~~ by a portion of the contact electrode metal ~~207'~~ and a metal electrode ~~214'~~, and the first comb-shaped pixel metal electrode ~~71~~ 271 was connected to a drain region ~~216~~ by a portion of the contact electrode metal ~~207'~~.

At this point, the source segmented wiring lines ~~209'~~ and ~~209''~~, which had been previously severed, were connected together on the gate wiring line ~~203'~~ by the metal electrode ~~214'~~ via a portion of the contact electrode metal ~~207'~~.

Subsequently, a silica passivation film ~~217~~ of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film ~~205~~ and the SiN_x film ~~204~~ on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

An Al–Zr alloy was then vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode 272 was formed, thus producing a TFT array substrate 273 applicable to IPS mode transmissive liquid crystal display devices, with the use of three

photomasks (Figs. 24(a) and 24(b)).

Here, when the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer and part of the n-type layer was etched to the i-type layer, it was possible to simplify the TFT process.

In addition, forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to fabricate a TFT array substrate having stable characteristics.

When at least the gate wiring line metal film, the gate insulating film, and the semiconductor film were sequentially formed, it was possible to prevent contamination of the channel interfaces.

In the step of oxidation, by carrying out anodic oxidation, it was possible to form an insulating film having few pinholes, allowing fabrication of a TFT array substrate having little gate leakage.

Here, when the oxide films of the side surfaces of the gate electrodes were formed of anodic oxide films, it was possible to fabricate a TFT array substrate having excellent leakage characteristics.

Furthermore, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact electrode metal film layer, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring line, allowing fabrication of a TFT array substrate having few variations in characteristics.

When a contact electrode metal was formed between the semiconductor film and the source/drain electrodes, it was possible to fabricate a TFT array substrate having little internal resistance.

Moreover, when segments of each source segmented wiring line, which had been severed by the gate wiring lines, were interconnected together on the gate wiring lines by the contact electrode metal and the metal electrode, it was possible to fabricate a TFT array substrate having a low resistance of the source segmented wiring line.

When part of the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer, it was possible to omit the step of diffusing an n-type impurity.

Forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to minimize the influence of the substrate deformation.

Example 2-10

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-9 is described.

First, there were provided a TFT array substrate, similar to that of Example 2-9, fabricated using two masks, more specifically, a first TFT array substrate ~~223~~ including a first comb-shaped electrode group and a second comb-shaped electrode group ~~221~~ arranged in a matrix and a transistor group ~~22~~ that drives the first ~~electrodes~~ comb-shaped electrode group; and a second color filter substrate ~~226~~ including a color filter group ~~224~~ placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films ~~227~~.

Next, the first and second substrates ~~225~~ and ~~226~~ were arranged such that ~~the electrodes~~ <u>their respective alignment films</u> oppose one another, thus producing a cell having ~~an alignment direction twisted 90 degrees and~~ a gap of about 5 microns, which is created by spacers ~~228~~ and adhesives ~~229~~. Thereafter, a TN liquid crystal ~~230~~ was injected between the first and second substrates, and polarizers ~~231~~ and ~~232~~ were then arranged so as to have a crossed Nicols relation, thus completing a display device. ~~(A drawing of the present example is similar to that in Fig. 21 and thus is omitted.)~~

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 210.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

<u>Example 2-11</u>

In a manner similar to that described in Example 2-8, a transparent glass substrate ~~1~~ that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer ~~202~~, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer ~~203~~ for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate

insulating film layer ~~4~~, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film ~~205~~ not containing impurities and an amorphous silicon (n+a-Si) film ~~206~~ containing an n-type impurity to 50 nm and 50 nm, respectively, and then a first resist pattern ~~208~~ for the first photolithography was formed by a conventional method.

Thereafter, the n+a-Si film ~~206~~, the i-type a-Si film ~~205~~, the SiN_x film ~~204~~, and the Al–Zr film ~~203~~ were sequentially etched, thereby forming a first pattern ~~210~~ including a gate electrode ~~203'~~ or a gate wiring line ~~203''~~, a source segmented wiring line ~~209'~~, a gate insulating film layer ~~204'~~, and a semiconductor film ~~(205' and 206')~~ which were stacked.

Next, the gate electrode ~~203'~~ and the gate wiring line ~~203''~~ were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films ~~211~~, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a Ti metal film, serving as a contact metal film layer ~~207~~, was vapor deposited by sputtering to a film thickness of about 100 nm, and subsequently an Al–Zr film, serving as a metal electrode film, was vapor deposited by sputtering to a film thickness of about 100 nm. The contact metal film layer and the metal electrode film are to be connected to source regions and to first comb-shaped pixel metal electrodes connected to drain regions, and to connect together segments of each severed source segmented wiring line.

Thereafter, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a

conventional method. Subsequently, part of the transparent conductive film ~~12'~~, the contact metal film layer ~~electrode 7'~~, and the n+a-Si film ~~6'~~ on the gate electrode were sequentially etched away through to the i-type a-Si film, thus forming channel regions. ~~and the~~ The source segmented wiring line ~~206'~~ was connected to a source region ~~13~~ by a portion of the contact electrode metal ~~207'~~ and a metal electrode ~~14''~~, and the first comb-shaped pixel metal electrode ~~81~~281 was connected to a drain region ~~16~~ by a portion of the contact electrode metal ~~7'~~.

At this point, the source segmented wiring lines ~~9'~~ and ~~9''~~, which had been previously severed, were connected together on the gate wiring line ~~3'~~ by the two-layered structure composed of the metal electrode ~~14''~~ and a portion of the contact electrode metal ~~7'~~.

Subsequently, a silica passivation film ~~17~~ of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film ~~5~~ and the SiN_x film 4 on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

Finally, an Al–Zr alloy was once again vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode ~~82~~282 was formed, thus producing a TFT array substrate ~~83~~283 applicable to IPS mode transmissive liquid crystal display devices, with the use of three photomasks (Figs. 25(a) and 25(b)).

Consequently, because at least segments of each source segmented wiring line were connected together by the two-layered structure composed

of the metal electrode and the contact electrode metal, it was possible to reduce the resistance of the source segmented wiring line, allowing fabrication of a TFT array substrate having excellent image display characteristics.

Example 2-12

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-11 is described.

First, there were provided a TFT array substrate, similar to that of Example ~~2-9~~ 2-11, fabricated using two masks, more specifically, a first TFT array substrate ~~223~~ including a first comb-shaped electrode group ~~221~~ and a second comb-shaped electrode group arranged in a matrix and a transistor group ~~222~~ that drives the first comb-shaped electrode group ~~electrode~~; and a second color filter substrate ~~226~~ including a color filter group ~~224~~ placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films ~~227~~.

Next, the first and second substrates ~~223~~ and ~~226~~ were arranged such that ~~the electrodes~~ their respective alignment films oppose one another, thus producing a cell having ~~an alignment direction twisted 90 degrees and~~ a gap of about 5 microns, which is created by spacers ~~228~~ and adhesives ~~229~~. Thereafter, a TN liquid crystal ~~230~~ was injected between the first and second substrates, and polarizers ~~231~~ and ~~232~~ were then arranged so as to

have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability. ~~(A drawing of the present example is similar to that in Fig. 21 and thus is omitted.)~~

INDUSTRIAL APPLICABILITY

As has been explained above, according to the present invention, it is possible to fabricate an electrical circuit board having X-Y wiring lines that intersect one another in the plane, with extremely high productivity. Such an electrical circuit board is applicable in a wide range of electronic device applications. In addition, the TFT array substrates in accordance with the present invention, to which such an electrical circuit board is applied, can be fabricated with the use of two photomasks, and therefore a substantial reduction in the fabrication costs of TFT array substrates is achieved. Moreover, using such TFT array substrates produces the advantageous effect of providing liquid crystal display devices at a lower cost. Thus, the value of the present invention to industry is considerable.

15. A method of fabricating a bottom-gate TFT array substrate comprising:

(A) sequentially depositing at least a G-S metal film layer, a gate insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines;

(B), after step (A), by photolithography, using a first resist pattern, etching the layers through to the surface of the insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines;

(C), after step (B), [etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form on the semiconductor film, and] oxidizing side surfaces of the gate electrodes and side surfaces of the gate wiring lines to form an electrically insulating metal oxide film;

[(E)] (D), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and

[(F)] (E), after step [(E)] (D), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a predetermined pattern to form pixel electrodes and [channel regions exposed by the etching] etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form channel regions on the semiconductor film.

16. The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein the oxidation of the side surfaces of the gate electrodes and the side surfaces of the gate wiring lines is carried out by anodic oxidation.

17. The method of fabricating a bottom-gate TFT array substrate according to claim 15 wherein:

the semiconductor film layer has a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and

step [(F)] (E) of etching the contact metal film of the gate electrode section pattern is carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous silicon layer.

18. The method of fabricating a bottom-gate TFT array substrate

according to claim 15, wherein in place of the transparent conductive film layer in step [(E)] (D), a light reflective conductive film layer is deposited.

24. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the reflective pixel metal electrodes has a two-layered structure composed of a contact [metal electrode] electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact [metal electrode] electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact [metal electrode] electrode metal and a metal electrode.

26. The bottom-gate TFT array substrate according to claim 24, wherein part of each source segmented wiring line has a two-layered structure composed of a contact [electrode metal film] metal film and an aluminum-based metal electrode film.

27. The bottom-gate TFT array substrate according to claim 24, wherein the gate insulating film and the semiconductor film are formed between the gate electrode metal and the contact [metal electrode] electrode metal.

28. The bottom-gate TFT array substrate according to claim 24, wherein the source segmented wiring lines are severed by the gate wiring

lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact [metal electrode] electrode metal and the metal electrode.

31. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact [electrode metal film] metal film and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact [electrode metal film] metal film, and the semiconductor film, using a second pattern.

36. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each having a two-layered structure composed of a contact [metal electrode] electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact [metal electrode] electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact [metal electrode] electrode metal and a

metal electrode; and

a color filter substrate having a color filter side on which a counter transparent electrode is formed;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

39. A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact [electrode metal film] metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact [electrode metal film] metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the [bottom-gate TFT array] first substrate;

forming an alignment film on a surface of a counter electrode side of a second color filter substrate having a counter transparent electrode formed thereon;

adhering and fixing the [bottom-gate TFT array substrate and the color filter substrate] first and second substrates at the periphery thereof such that the substrates are arranged with the two

alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

41. The method of fabricating a liquid crystal display device according to claim 39, wherein the metal electrode and the contact [metal electrode] electrode metal are formed in a single layer with a same material.

42. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized;

each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

44. The bottom-gate TFT array substrate according to claim 42, wherein the first comb-shaped pixel electrodes and part of each source segmented wiring line have a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact [electrode metal film] metal film layer, and a metal electrode film.

49. A method of fabricating a bottom-gate TFT array substrate

comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact [electrode metal film] metal film layer on a surface of an insulating substrate;

by photolithography, sequentially etching the contact [electrode metal film] metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes;

forming a metal electrode film; and

by photolithography, sequentially etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern.

57. A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact [electrode metal film] metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact [electrode metal film] metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern;

forming an alignment film on the [bottom-gate TFT array] first

substrate;

forming an alignment film on a surface of a second color filter substrate;

adhering and fixing the [bottom-gate TFT array substrate and the color filter substrate] first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

58. The method of fabricating a liquid crystal display device according to claim 57, further comprising:

after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film; and

using the passivation film as a mask, etching the metal electrode film, the contact [electrode metal film] metal film layer, the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

60. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact [metal electrode] electrode metal and another metal electrode film and is connected

to a drain region of a corresponding TFT by the contact [metal electrode] electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact [metal electrode] electrode metal and a metal electrode.

62. The bottom-gate TFT array substrate according to claim 60, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact [electrode metal film] metal film layer, and a metal electrode film.

63. The bottom-gate TFT array substrate according to claim 60, wherein the contact [metal electrode] electrode metal is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

64. The bottom-gate TFT array substrate according to claim 60, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact [metal electrode] electrode metal and the metal electrode.

67. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes;

forming a contact [electrode metal film] metal film layer and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern.

72. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a contact [metal electrode] electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact [metal electrode] electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact [metal electrode] electrode metal and a metal electrode; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

75. A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact [electrode metal film] metal film layer and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern;

forming an alignment film on the [bottom-gate TFT array] first substrate;

forming an alignment film on a surface of a counter electrode side of a second color filter substrate;

adhering and fixing the [bottom-gate TFT array substrate and the color filter substrate] first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

77. The method of fabricating a liquid crystal display device according to claim 75, wherein the metal electrode and the contact [metal electrode] electrode metal are formed in a single layer with a same material.

78. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a

semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped [opposing] pixel electrodes are formed with [an insulating] a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate.

80. The bottom-gate TFT array substrate according to claim 78, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

85. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact [electrode metal film] metal film layer on a surface of an insulating substrate;

by photolithography, sequentially etching the contact [electrode metal film] metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern; and

forming second comb-shaped [opposing] pixel electrodes using a third pattern with [an insulating] a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate.

90. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped [opposing] pixel electrodes formed with [an insulating] a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

93. A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming

at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact [electrode metal film] metal film layer on a surface of an insulating substrate; by photolithography, sequentially etching the contact [electrode metal film] metal film layer, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped [opposing] pixel electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate;

forming an alignment film on the [bottom-gate TFT array] first substrate;

forming an alignment film on a surface of a color filter side of a second color filter substrate;

adhering and fixing the [bottom-gate TFT array substrate and the color filter substrate] first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

94. The method of fabricating a liquid crystal display device according to claim 93, further comprising, after the formation of the second comb-shaped [opposing] pixel electrodes, covering at least part of each

second comb-shaped [opposing] pixel electrode by a passivation film.

96. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate electrodes, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact electrode metal;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped [opposing] pixel electrodes are formed with [an insulating] a passivation film disposed between the second-comb shaped [opposing] pixel electrodes and the substrate.

98. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact [electrode metal film] metal film layer and a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern; and

forming second comb-shaped [opposing] pixel electrodes, using a third pattern, with [an insulating] a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate.

99. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped [opposing] pixel electrodes formed with [an insulating] a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

100. A method of fabricating a liquid crystal display device comprising:

fabricating a first bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact [electrode metal film] metal film layer and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact [electrode metal film] metal film layer, and the semiconductor film, using a second pattern; and forming second comb-shaped [opposing] pixel electrodes, using a third pattern, with [an insulating] a passivation film disposed between the second comb-shaped [opposing] pixel electrodes and the substrate;

forming an alignment film on the [bottom-gate TFT array] first substrate;

forming an alignment film on a surface of a color filter side of a second color filter substrate;

adhering and fixing the [bottom-gate TFT array substrate and the color filter substrate] first and second substrates at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

101. The method of fabricating a liquid crystal display device according to claim 100, further comprising covering at least part of each second

comb-shaped [opposing] pixel electrode by a passivation film.

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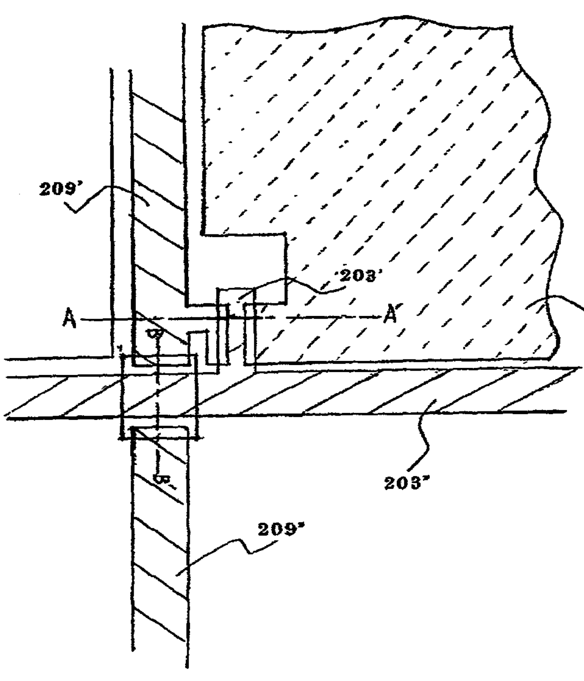

(57) Abstract: A TFT array substrate used for a liquid-crystal display panel is disclosed of which the manufacturing process is simplified and the manufacturing cost is reduced by reducing the number of masks used in manufacturing the TFT array substrate. A gate wiring metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film are formed on a substrate surface. The contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring metal film are sequentially etched by photolithography using a first pattern, and the gate wiring and a part of the side of the gate wiring metal film pattern which is to serve as a gate electrode are oxidized. A transparent conductive film is formed. The transparent conductive film, the contact electrode metal film, and a part of the semiconductor film are sequentially etched by photolithography using a second pattern.

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ELECTRICAL CIRCUIT BOARD AND TFT ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME

TECHNICAL FIELD

The present invention relates to an innovative structure for electrical circuit boards having various applications, to TFT array substrates to which such electrical circuit boards are applied, and to liquid crystal display devices utilizing such TFT array substrates. The invention further relates to the fabrication methods of such electrical circuit boards, TFT array substrates, and liquid crystal display devices.

BACKGROUND ART

Conventionally, fabricating a TFT (Thin Film Transistor) array substrate for a color liquid crystal display device requires five to nine photomasks. As the number of photomasks to be used is increased, the number of the fabrication steps increases accordingly, and therefore the fabrication becomes complicated, making it difficult to reduce the fabrication cost.

Meanwhile, a technique for reducing the number of photomasks used in the fabrication process of a diode array substrate to two has been proposed (Published Japanese Translation of PCT International Publication for Patent Application No. 62-502361). However, the performance of diode array substrates is inferior to that of TFT (Thin Film Transistor) array substrates, and therefore the diode array substrate is not suitable for use in

color televisions.

DISCLOSURE OF THE INVENTION

In view of the foregoing, it is a principal object of the invention to provide an innovative structure that allows for reduction in the number of photomasks necessary for fabricating a TFT array substrate.

(1) A first aspect of the present invention for achieving this object relates to a structure for electrical circuit boards applicable to semiconductor integrated circuits and the like. The first aspect of the present invention includes the following.

There is provided an electrical circuit board comprising; X wiring lines and Y segmented wiring lines, each of the wiring lines being formed of a same conductive metal film and in a same plane on an insulating substrate and the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines; wherein top and side surfaces of the X wiring lines are covered with an insulating film; and segments of each of the Y segmented wiring lines are electrically connected together by a Y segmented wiring line-connecting electrode formed on the insulating film.

With this construction, it is possible to build an X-Y wiring line intersection type electrical circuit, which allows an electric current to pass through independently, into an extremely thin plane, and therefore it is also possible to realize a multi-level integrated circuit. Hence, this construction is very compatible with semiconductor devices, and employing this construction allows remarkable increase in the degree of integration of

semiconductor circuits and the like.

In this construction, the insulating film of at least the side surfaces of the X wiring lines may be a metal oxide film formed by oxidizing the conductive metal film. In addition, the metal oxide film may be an anodic oxide film formed by anodic oxidation. The anodic oxide film is preferable because such a film is thin and provides excellent insulation.

The electrical circuit board having the above-described construction may be fabricated by the following fabrication method, with great productivity. Specifically, the method comprising: a first step of depositing a conductive metal film layer over an insulating substrate; a second step of etching the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines; a third step, after the second step, of oxidizing top and side surfaces of the X wiring lines to cover the top and side surfaces by an insulating metal oxide film; and a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

In this fabrication method, the third step of oxidizing the X wiring lines may be carried out by anodic oxidation. The anodic oxidation allows only the X wiring lines to be selectively and efficiently oxidized.

The electrical circuit board having the above-described construction

may also be fabricated by the following method, with great productivity. Specifically, the method comprising: a first step of sequentially depositing at least a conductive metal film layer and an insulating film layer over an insulating substrate; a second step of etching layers including the insulating film layer and the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines; a third step, after the second step, of oxidizing side surfaces of the X wiring lines to cover the side surfaces by an insulating metal oxide film; and a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

In this fabrication method also, the third step of oxidizing the side surfaces of the X wiring lines may be carried out by anodic oxidation.

(2) A second aspect of the present invention relates to a bottom-gate TFT array substrate to which the above-described electrical circuit is applied, and includes the following.

There is provided a bottom-gate TFT array substrate comprising: gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film; a gate insulating film stacked on each of the gate electrodes; a semiconductor film stacked on the

gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions; source contact electrodes stacked on the source regions of the semiconductor film; drain contact electrodes stacked on the drain regions of the semiconductor film; pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes; gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film; source segmented wiring lines formed in a same plane as the gate wiring lines, each of the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines.

With this construction, it is possible to provide a bottom-gate TFT array substrate with excellent reliability.

In this construction, the pixel electrodes and the source wiring line-connecting electrodes may be composed of a same transparent conductive film material.

Further, the substrate may be constructed such that a source segmented wiring line section pattern has a five-layered structure composed of the source segmented wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the source segmented wiring lines are located at the bottom of the five-layered structure; a gate wiring line section pattern has a five-layered structure

composed of the gate wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the gate wiring lines are located at the bottom of the five-layered structure; and the source segmented wiring lines and the gate wiring lines are in the same plane on the substrate.

In addition, the insulating film of at least the side surfaces of the gate wiring lines may be composed of an oxide film formed from the conductive metal film.

Moreover, the oxide film may be an anodic oxide film formed by anodic oxidation.

The substrate may also be constructed such that the semiconductor film has a two-layered structure composed of an i-type amorphous silicon layer and an n-type amorphous silicon layer.

Furthermore, in place of the transparent conductive film material, a light reflective conductive film material may be used. Thereby, it is possible to construct a bottom-gate TFT array substrate for reflective devices.

The above-described bottom-gate TFT array substrate may be fabricated by the following fabrication method, with great productivity.

Specifically, the method comprising: (A) sequentially depositing at least a G-S metal film layer, a gate insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines; (B), after step (A), by photolithography, using a first resist pattern, etching the layers through to

the surface of the insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines; (C), after step (B), etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form on the semiconductor film, and oxidizing side surfaces of the gate electrodes and side surfaces of the gate wiring lines to form an electrically insulating metal oxide film; (E), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and (F), after step (E), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a predetermined pattern to form pixel electrodes and channel regions exposed by the etching.

In this fabrication method, the oxidation of the side surfaces of the gate wiring lines may be carried out by anodic oxidation.

In addition, the semiconductor film layer may have a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and step (F) of etching the contact metal film of the gate electrode section pattern may be carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous silicon layer.

Furthermore, in place of the transparent conductive film layer in step (E), a light reflective conductive film layer may be deposited.

(3) A third aspect of the present invention relates to a liquid crystal display device utilizing a bottom-gate TFT array substrate, and includes the following.

There is provided a liquid crystal display device comprising; a bottom-gate TFT array substrate including gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film; a gate insulating film stacked on the gate electrodes; a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions; source contact electrodes stacked on the source regions of the semiconductor film; drain contact electrodes stacked on the drain regions of the semiconductor film; pixel electrodes connected to the drain regions of the semiconductor film by

the drain contact electrodes; gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film; source segmented wiring lines formed in a same plane as the gate wiring lines, the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines; and a counter substrate; wherein the TFT array substrate and the counter substrate are opposed to each other with a surface on which the TFTs are being formed facing inside and with a predetermined gap therebetween, a liquid crystal being held in the gap.

It is possible to further add the following to this construction. Specifically, the construction may be such that a surface of the TFT array substrate is protected by a passivation film. In addition, the passivation film may be one selected from the group consisting of a silica film and a silicon nitride film.

Furthermore, the pixel electrodes may be composed of a transparent metal film.

Moreover, the pixel electrodes may be composed of a light reflective metal film.

(4) A fourth aspect of the present invention (twenty-fourth to thirtieth embodiments) relates to a bottom-gate TFT array substrate, and includes the following.

(Twenty-fourth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the reflective pixel metal electrodes has a two-layered structure composed of a contact metal electrode and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact metal electrode; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode.

(Twenty-fifth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the reflective pixel metal electrode group is one selected from the group consisting of aluminum and an aluminum-based alloy.

(Twenty-sixth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that part of each source segmented wiring line has a two-layered structure composed of a contact electrode metal film and an aluminum-based metal electrode film.

(Twenty-seventh embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the gate insulating film and the semiconductor film are formed between the gate electrode metal and the

contact metal electrode.

(Twenty-eighth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact metal electrode and the metal electrode.

(Twenty-ninth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n+-type layer.

(Thirtieth embodiment)

The bottom-gate TFT array substrate according to the twenty-fourth embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

(5) A fifth aspect of the present invention (thirty-first to thirty-fifth embodiments) includes the following.

(Thirty-first embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a

contact electrode metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

(Thirty-second embodiment)

In the fabrication method according to the thirty-first embodiment, the metal electrode film may be an aluminum or aluminum-based alloy film.

(Thirty-third embodiment)

The fabrication method according to the thirty-first embodiment may further comprise forming a silica-based undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Thirty-fourth embodiment)

In the fabrication method according to the thirty-first embodiment, at least an aluminum-based alloy film may be formed for the gate wiring line metal film.

(Thirty-fifth embodiment)

In the fabrication method according to the thirty-first embodiment, the oxidation may be carried out, by anodic oxidation, in a neutral solution.

(6) A sixth aspect of the present invention (thirty-sixth to thirty-eighth embodiments) includes the following.

(Thirty-sixth embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each having a two-layered structure

composed of a contact metal electrode and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact metal electrode; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode; and a color filter substrate having a color filter side on which a counter transparent electrode is formed; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Thirty-seventh embodiment)

The liquid crystal display device according to the thirty-sixth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Thirty-eighth embodiment)

The liquid crystal display device according to the thirty-seventh embodiment may be such that the passivation film is an inorganic substance.

(7) A seventh aspect of the present invention (thirty-ninth to forty-first embodiments) includes the following.

(Thirty-ninth embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a

semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; forming an alignment film on the bottom-gate TFT array substrate; forming an alignment film on a surface of a counter electrode side of a color filter substrate having a counter transparent electrode formed thereon; adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Fortieth embodiment)

The fabrication method according to the thirty-ninth embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

(Forty-first embodiment)

The fabrication method according to the thirty-ninth embodiment may be such that the metal electrode and the contact metal electrode are formed in a single layer with a same material.

(8) An eighth aspect of the present invention (forty-second to forty-eighth embodiments) includes the following.

(Forty-second embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized; each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

(Forty-third embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the oxide film of the side surfaces of the gate electrodes and of the first comb-shaped pixel electrodes is an anodic oxide film.

(Forty-fourth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the first comb-shaped pixel electrodes and part of each source segmented wiring line have a five-layered structure composed of a gate wiring line metal film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

(Forty-fifth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the contact electrode metal is formed to connect each of the comb-shaped electrodes to the semiconductor film.

(Forty-sixth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines and the first comb-shaped electrodes, and segments of each source segmented wiring line are interconnected together on the gate wiring lines and the first comb-shaped electrodes by a contact electrode metal and the metal electrode.

(Forty-seventh embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

(Forty-eighth embodiment)

The bottom-gate TFT array substrate according to the forty-second embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and a gate wiring line metal film.

(9) A ninth aspect of the present invention (forty-ninth to fifty-third embodiments) includes the following.

(Forty-ninth embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially

etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

(Fiftieth embodiment)

The fabrication method according to the forty-ninth embodiment may be such that portions to be formed into the gate wiring lines, the gate electrodes, and the first comb-shaped pixel electrodes are simultaneously etched.

(Fifty-first embodiment)

The fabrication method according to the forty-ninth embodiment may further comprise forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Fifty-second embodiment)

The fabrication method according to the forty-ninth embodiment may be such that at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

(Fifty-third embodiment)

The fabrication method according to the forty-ninth embodiment may be such that the oxidation is carried out by anodic oxidation.

(10) A tenth aspect of the present invention (fifty-fourth to fifty-sixth embodiments) includes the following.

(Fifty-fourth embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes, gate wiring lines, and first comb-shaped electrodes, at least side surfaces of the gate electrodes, of the gate wiring lines, and of the first comb-shaped electrodes being oxidized; second comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Fifty-fifth embodiment)

The liquid crystal display device according to the fifty-fourth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Fifty-sixth embodiment)

The liquid crystal display device according to the fifty-fifth embodiment may be such that the passivation film is an inorganic substance.

(11) An eleventh aspect of the present invention (fifty-seventh to fifty-ninth embodiments) includes the following.

(Fifty-seventh embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; forming an alignment film on the bottom-gate TFT array substrate; forming an alignment film on a surface of a color filter substrate; adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Fifty-eighth embodiment)

The fabrication method according to the fifty-seventh embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film; and using the passivation film as a mask, etching the metal electrode film, the contact electrode metal film,

the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

(Fifty-ninth embodiment)

The fabrication method according to the fifty-eighth embodiment may be such that the passivation film is a silica film or a silicon nitride film.

(12) A twelfth aspect of the present invention (sixtieth to sixty-sixth embodiments) includes the following.

(Sixtieth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact metal electrode and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact metal electrode; and each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode.

(Sixty-first embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that an aluminum-based metal is used for the gate electrodes, and the insulating film of the side surfaces is an anodic oxide film.

(Sixty-second embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

(Sixty-third embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that the contact metal electrode is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

(Sixty-fourth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact metal electrode and the metal electrode.

(Sixty-fifth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

(Sixty-sixth embodiment)

The bottom-gate TFT array substrate according to the sixtieth embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

(13) A thirteenth aspect of the present invention (sixty-seventh to

seventy-first embodiments) includes the following.

(Sixty-seventh embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact electrode metal film and a metal electrode film; and by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

(Sixty-eighth embodiment)

The fabrication method according to the sixty-seventh embodiment may be such that the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched through to the i-type layer.

(Sixty-ninth embodiment)

The fabrication method according to the sixty-seventh embodiment may further comprise forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Seventy embodiment)

The fabrication method according to the sixty-seventh embodiment may be such that at least the gate wiring line metal film, the gate insulating

film, and the semiconductor film are sequentially formed.

(Seventy-first embodiment)

The fabrication method according to the sixty-seventh embodiment may be such that the oxidation is carried out by anodic oxidation.

(14) A fourteenth aspect of the present invention (seventy-second to seventy-fourth embodiments) includes the following.

(Seventy-second embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a contact metal electrode and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact metal electrode; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Seventy-third embodiment)

The liquid crystal display device according to the seventy-second embodiment may be such that at least part of the TFT array is covered with

a passivation film.

(Seventy-fourth embodiment)

The liquid crystal display device according to the seventy-second embodiment may be such that the passivation film is an inorganic substance.

(15) A fifteenth aspect of the present invention (seventy-fifth to seventy-seventh embodiments) includes the following.

(Seventy-fifth embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; forming an alignment film on the bottom-gate TFT array substrate; forming an alignment film on a surface of a counter electrode side of a color filter substrate; adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a

specified liquid crystal between the first and second substrates.

(Seventy-sixth embodiment)

The fabrication method according to the seventy-fifth embodiment may further comprise, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

(Seventy-seventh embodiment)

The fabrication method according to the seventy-fifth embodiment may be such that the metal electrode and the contact metal electrode are formed in a single layer with a same material.

(16) A sixteenth aspect of the present invention (seventy-eighth to eighty-fourth embodiments) includes the following.

(Seventy-eighth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized; each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and the second comb-shaped opposing electrodes are formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

(Seventy-ninth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the oxide film of the side surfaces of the gate electrodes is an anodic oxide film.

(Eightieth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

(Eighty-first embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the contact electrode metal is formed between the semiconductor film and a source electrode and between the semiconductor film and a drain electrode.

(Eighty-second embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by a contact electrode metal and the metal electrode.

(Eighty-third embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

(Eighty-fourth embodiment)

The bottom-gate TFT array substrate according to the seventy-eighth embodiment may be such that an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

(17) A seventeenth aspect of the present invention (eighty-fifth to eighty-ninth embodiments) includes the following.

(Eighty-fifth embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes using a third pattern with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

(Eighty-sixth embodiment)

The fabrication method according to the eighty-fifth embodiment may be such that the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched.

(Eighty-seventh embodiment)

The fabrication method according to the eighty-fifth embodiment may further comprise forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

(Eighty-eighth embodiment)

The fabrication method according to the eighty-fifth embodiment may be such that at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

(Eighty-ninth embodiment)

The fabrication method according to the eighty-fifth embodiment may be such that the oxidation is carried out by anodic oxidation.

(18) An eighteenth aspect of the present invention (ninetieth to ninety-second embodiments) includes the following.

(Embodiment ninetieth)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped opposing electrodes formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the

electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(Ninety-first embodiment)

The liquid crystal display device according to the ninetieth embodiment may be such that at least part of the TFT array is covered with a passivation film.

(Ninety-second embodiment)

The liquid crystal display device according to the ninety-first embodiment may be such that the passivation film is an inorganic substance.

(19) A nineteenth aspect of the present invention (ninety-third to ninety-fifth embodiments) includes the following.

(Ninety-third embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode

metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped opposing electrodes and the substrate; forming an alignment film on the bottom-gate TFT array substrate; forming an alignment film on a surface of a color filter side of a color filter substrate; adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Ninety-fourth embodiment)

The fabrication method according to the ninety-third embodiment may further comprise, after the formation of the second comb-shaped opposing electrodes, covering at least part of each second comb-shaped opposing electrode by a passivation film.

(Ninety-fifth embodiment)

The fabrication method according to the ninety-third embodiment may be such that the passivation film is a silica film or a silicon nitride film.

(20) A twentieth aspect of the present invention (ninety-sixth and ninety-seventh embodiments) includes the following.

(Ninety-sixth embodiment)

There is provided a bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein: at least side surfaces of gate

electrodes and side surfaces of the gate wiring lines are oxidized; each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and is connected to a drain region of a corresponding TFT; each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and the second comb-shaped opposing electrodes are formed with an insulating film disposed between the second-comb shaped opposing electrodes and the substrate.

(Ninety-seventh embodiment)

The bottom-gate TFT array substrate according to the ninety-sixth embodiment may be such that at least segments of each source segmented wiring line are connected together by a two-layered structure composed of the metal electrode and a contact electrode metal.

(21) A twenty-first aspect of the present invention (ninety-eighth embodiment) includes the following.

(Ninety-eighth embodiment)

There is provided a method of fabricating a bottom-gate TFT array substrate comprising: forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode

metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes, using a third pattern, with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

(22) A twenty-second aspect of the present invention (ninety-ninth embodiment) includes the following.

(Ninety-ninth embodiment)

There is provided a liquid crystal display device comprising: a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and being connected to a drain region of a corresponding TFT; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped opposing electrodes formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; and a color filter substrate having a color filter side; wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

(23) A twenty-third aspect of the present invention (hundredth and hundred-first embodiments) includes the following.

(Hundredth embodiment)

There is provided a method of fabricating a liquid crystal display device comprising: fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes, using a third pattern, with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; forming an alignment film on the bottom-gate TFT array substrate; forming an alignment film on a surface of a color filter side of a color filter substrate; adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and injecting a specified liquid crystal between the first and second substrates.

(Hundred-first embodiment)

The fabrication method may further comprise covering at least part of each second comb-shaped opposing electrode by a passivation film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view illustrating a process step for fabricating an electrical circuit board in accordance with Example 1-1 of the present invention.

Fig. 2 is a plan view showing the state of the substrate surface that has been etched using a first resist pattern in accordance with Example 1-1 of the present invention.

Fig. 3 is a plan view showing the state where a conductive film layer is deposited on the entire surface of the substrate in accordance with Example 1-1 of the present invention.

Fig. 4 is a plan view showing the state where the conductive film layer on the substrate has been processed into a predetermined pattern (Y segmented wiring line-connecting electrodes) in accordance with Example 1-1 of the present invention.

Figs. 5(a) and 5(b) are schematic cross-sectional views illustrating a process step for fabricating a TFT array in accordance with Example 2-1 of the present invention.

Figs. 6(a) and 6(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Fig. 7 is a schematic top plan view of Fig. 6(b).

Figs. 8(a) and 8(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Figs. 9(a) and 9(b) are schematic cross-sectional views illustrating a

process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Figs. 10(a) and 10(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Figs. 11(a) and 11(b) are schematic cross-sectional views illustrating a process step for fabricating the TFT array in accordance with Example 2-1 of the present invention.

Fig. 12 is a schematic plan view of the TFT array substrate in accordance with Example 2-1.

Fig. 13 is a schematic cross-sectional view illustrating a liquid crystal display device in accordance with Example 2-2 of the present invention.

Figs. 14(a) and 14(b) are views illustrating a process step for fabricating a TFT array in accordance with Example 2-3 of the present invention.

Figs. 15(a) and 15(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 16(a) and 16(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 17(a) and 17(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 18(a) and 18(b) are views illustrating a process step for

fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 19(a) and 19(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Figs. 20(a) and 20(b) are views illustrating a process step for fabricating the TFT array in accordance with Example 2-3 of the present invention.

Fig. 21 is a schematic cross-sectional view illustrating a liquid crystal display device in accordance with Example 2-4 of the present invention.

Figs. 22(a) and 22(b) are schematic cross-sectional views of a TFT in accordance with Example 2-5 of the present invention.

Figs. 23(a) and 23(b) are schematic cross-sectional views of a TFT in accordance with Example 2-7 of the present invention.

Figs. 24(a) and 24(b) are schematic cross-sectional views of a TFT in accordance with Example 2-9 of the present invention.

Figs. 25(a) and 25(b) are schematic cross-sectional views of a TFT in accordance with Example 2-11 of the present invention.

Fig. 26 is a view showing the entire TFT array substrate in accordance with Example 2-1 of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention is described in more detail below with reference to examples thereof.

<u>Example 1-1</u>

A transparent glass substrate (insulating substrate) 101 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film layer, serving as an undercoat film layer 102, was deposited by CVD to a thickness of 0.4 microns. Subsequently, an Al–Zr (97:3) alloy film layer, serving as a metal film layer 103 for forming X wiring lines and Y segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Further, a SiN_X film, serving as an insulating film layer 104, was deposited by plasma enhanced CVD to 150 nm (Fig. 1).

Next, by photolithography using a first resist pattern 105 (Fig. 1), the layers were etched from the top of the insulating film layer 104 through to the undercoat film layer 102, to form X wiring lines 106 and Y segmented wiring lines 107 in a pattern on the substrate, the Y segmented wiring lines being severed by the X wiring lines at the intersections of the X wiring lines and the Y segmented wiring lines and being spaced apart from the X wiring lines (Fig. 2).

Then, by immersing the entire substrate in an electrolyte using ammonium borate and having a pH of about 7 and passing an electric current only through the X wiring lines from the periphery of the substrate (anodic oxidation), the side surfaces of the X wiring lines were oxidized, thus forming insulating metal oxide films 106' (mainly composed of Al_2O_3) on the side surfaces of the X wiring lines.

Subsequently, a conductive film layer 108 composed of, for example, indium tin oxide (ITO) was deposited on top of the insulating film layer 104 over the entire surface of the substrate so as to fill the space between the X wiring lines and the Y segmented wiring lines (Fig. 3). Thereafter,

unwanted areas of the conductive film on the insulating film were etched using a second resist pattern, as is shown in Fig. 4, to form Y segmented wiring line-connecting electrodes 109. As a result of this etching, electrical conduction between adjacent Y segmented wiring lines arranged parallel to one another is prevented and electrical conduction (connection) between segments of each Y segmented wiring line severed by the X wiring lines at the intersections of the X wiring lines and the Y segmented wiring lines is able to be realized by the Y segmented wiring line-connecting electrode 109, thus completing an electrical circuit board in accordance with Example 1-1 having such a structure.

<u>Example 1-2</u>

In Example 1-2, an insulating film layer 104 was not deposited. By using the above-described first resist pattern 105, a metal film layer 103 was etched to an undercoat film layer 102, thus forming X wiring lines and Y segmented wiring lines with no insulating films stacked thereon.

Subsequently, in a manner similar to that described in foregoing Example 1-1, the X wiring lines were oxidized by anodic oxidation to cover the side surfaces and top surfaces thereof by oxide films, mainly composed of Al_2O_3. It should be noted that in Example 1-2 both the top and side surfaces of the X wiring lines were oxidized in a manner similar to that described in the foregoing Example 1-1 because the metal film layer 103 was not covered by the insulating film layer 104 as was the case with Example 1-1.

Next, a conductive film layer (for example, ITO, Al, or the like) was

deposited on the entire surface of the substrate, and then using a second resist pattern, unwanted areas of the conductive film layer were etched away in a manner similar to that described in Example 1-1. Thereby, an electrical circuit board in accordance with Example 1-2 was completed in which there is no connection between adjacent Y segmented wiring lines arranged parallel to one another and in which segments of each Y segmented wiring line severed at the intersections of the X wiring lines and the Y segmented wiring lines are connected together by the conductive film.

It should be noted that in Examples 1-1 and 1-2 the surface of the metal film was oxidized by anodic oxidation because this method allows insulating films, formed from the metal oxide film, to be selectively formed only on the X wiring lines, providing superior productivity.

It should also be understood that in the foregoing Fig. 4, the connecting electrodes were formed in a belt shape lying along the Y segmented wiring lines, but the shape is not limited thereto. For example, the shape of the second resist pattern may be changed so as to form a square- or circle-shaped connecting electrode pattern that covers only the intersections of the X wiring lines and the Y segmented wiring lines.

Example 2-1

A transparent glass substrate (insulating substrate) 201 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to a thickness of 0.4 microns. Subsequently, an Al–Zr (97:3) alloy film, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source

segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Thereafter, a SiN_X film, serving as a gate insulating film layer 204, was deposited by plasma enhanced CVD to 150 nm. Then, as a semiconductor film layer 299, an amorphous silicon (i-type a-Si) film 205 not containing impurities and an amorphous silicon (n+a-Si) film 206 containing an n-type impurity were sequentially deposited to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer 207, was vapor deposited by sputtering to a film thickness of about 100 nm, and a first resist pattern 208 for the first photolithography was then formed by a conventional method (Figs. 5(a) and 5(b)).

Thereafter, the contact metal film layer 207 (Ti metal film), the n+a-Si film layer 206, the i-type a-Si film layer 205, the gate insulating film layer 204 (SiN_X film), and the G-S metal film layer 203 (Al–Zr film) were sequentially etched, thereby forming a first pattern 210 including a gate electrode 203' or a gate wiring line 203", source segmented wiring lines 209' and 209", a gate insulating film 204', the semiconductor film 299 (205' and 206'), and a contact metal film 207' which were stacked (Figs. 6(a) and 6(b)).

A schematic top plan view of Fig. 6(b) is shown in Fig. 7. As can be seen from Fig. 7, the gate wiring line 203" extends from the front to the end as viewed in the figure, and the source segmented wiring lines 209' and 209" extend in the direction orthogonal to the 203" (the horizontal direction as viewed in the figure). The source segmented wiring lines 209' and 209" are disconnected by the gate wiring line 203" crossing therebetween, and the gate wiring line 203" is spaced apart from each of the source segmented wiring lines 209' and 209" by a predetermined distance. It is preferable

that the distance of the space be made approximately equal to the total thickness of all the layers (etching depth).

It should be noted that Fig. 6(b) is a cross-sectional view taken along the line X–Y of Fig. 7.

Next, the gate electrode 203' and the gate wiring line 203" were selectively anodically oxidized in an electrolyte using ammonium borate and having a pH of about 7, to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the pattern (Figs. 8(a) and 8(b)).

Thereafter, a transparent conductive film 212, composed of an indium tin oxide (ITO) film, was vapor deposited by sputtering on the entire surface of the substrate to a film thickness of about 100 nm (Figs. 9(a) and 9(b)). The transparent conductive film 212 is to be connected to source regions and to pixel transparent electrodes 215, which are connected to drain regions, and also to connect together segments of each disconnected source segmented wiring line (i.e., serving as a source segmented wiring line-connecting electrode).

Subsequently, a second resist pattern 208' for the second photolithography (Figs. 10(a) and 10(b)) was formed by a conventional method. Then, part of the transparent conductive film 212, the contact metal film 207', and the n+a-Si film 206' on the gate electrode were sequentially etched away through to the i-type a-Si film 205', and the source segmented wiring line 209' was connected to a source region 213 by a portion of the contact electrode 207' and a transparent conductive film 214, and the pixel transparent electrode 215 was connected to a drain region 216 by a portion of the contact electrode 207' (Figs. 11(a) and 11(b)).

Thus, the disconnected source segmented wiring lines 209' and 209" are connected together by a transparent conductive film 214' and a portion of the contact metal film 207' on the gate wiring line 203" (Figs. 11(a) and 11(b)).

Finally, by using printing and baking a silica passivation film layer 217 of 300 nm was formed on the substrate, except for the periphery thereof, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, the peripheral portion of the stacked layers of the i-type a-Si film 205 and the gate insulating film layer 204 (SiN_x film), which is to be connected to external driving circuitry, was etched away to expose the gate G-S metal film 203 (see Fig. 26). Thereby, a TFT array substrate 218 (Fig. 26) applicable to transmissive liquid crystal display devices was produced.

Fig. 12 is an enlarged schematic plan view of a main portion of the TFT array substrate 218 produced in the present example. Fig. 11(a) is a cross-sectional view taken along the line A–A' of Fig. 12, and Fig. 11(b) is a cross-sectional view taken along the line B–B' of Fig. 18.

According to the present example described above, the gate wiring lines and the source segmented wiring lines are formed simultaneously in the same plane, and the side surfaces of the gate wiring lines are selectively oxidized by anodic oxidation for insulation. Segments of each source segmented wiring line, which has been disconnected by the gate wiring lines, are connected together by the contact metal film and the transparent conductive film that are stacked on each gate wiring line. Hence, the resistance of the source segmented wiring line is unlikely to increase substantially. In addition, with this structure, level differences on the

surface of the TFT array can be sufficiently minimized.

Further, in fabricating a TFT array substrate, conventional methods required five to seven photomasks; on the other hand, the fabrication method of the present example requires only two photomasks. Therefore, according to the method of the present example, it is possible to significantly reduce the fabrication costs of a TFT array substrate.

Moreover, for stacking layers on the substrate, by sequentially depositing the G-S metal film layer, the gate insulating film layer, and the semiconductor film layer, it is possible to fabricate a highly reliable bottom-gate TFT array substrate with little contamination at the interfaces of the channel portions.

For oxidation, by carrying out anodic oxidation using an electrolyte with a pH of 7, it is possible to efficiently and selectively oxidize only the side surfaces of the gate electrodes and the side surfaces of the gate wiring lines connected to the gate electrodes. In addition, this method allows for formation of high quality oxide films with no pinholes, thus achieving wiring lines with little gate leakage.

In this example, the source segmented wiring lines have a five-layered structure composed of the G-S metal film, the semiconductor film, the contact metal film, and the conductive film, and therefore the overall resistance of the source segmented wiring lines is reduced.

In addition, in this example, the gate insulting film and the semiconductor film are deposited between the G-S metal film (the gate electrodes, gate wiring lines, and source segmented wiring lines) and the contact metal film (contact electrodes), and therefore current leakage is less

likely to occur.

Furthermore, in this example, the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, whereby the contact resistance of the source and the drain can be reduced.

Since the undercoat film layer is disposed between the surface of the insulating substrate and the gate wiring line metal film, diffusion of impurities from the substrate can be prevented.

In the present example, a TFT array substrate for a transmissive device was produced; but it is also possible to produce a TFT array substrate for a reflective device, i.e., applicable to reflective liquid crystal display devices, by using a high-reflective metal film such as Al or an Al alloy in place of the transparent conductive film.

Example 2-2

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-1 is described with reference to Fig. 13.

First, there were provided a TFT array substrate, similar to that of Example 2-1, fabricated using two masks, more specifically, a first TFT array substrate 223 including a first electrode group 221 arranged in a matrix and a transistor group 222 that drives the first electrodes; and a color filter substrate 226 including a second electrode 225 and a color filter group 224 placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing

liquid crystal alignment films 227.

Next, the first and second substrates 223 and 226 were arranged such that their respective electrodes oppose one another, thus producing a cell having an alignment direction twisted 90 degrees and a gap of about 5 microns, created by spacers 228 and adhesives 229. Thereafter, a TN liquid crystal 230 was injected between the first and second substrates, and polarizers 231 and 232 were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images in the direction of the arrow A, by driving each transistor using video signals while lighting the entire display using a backlight 233. Here, after the step of fabricating the bottom-gate TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array by a passivation film, it was possible to fabricate a liquid crystal display device with high reliability.

In addition, for the passivation film, using a silica film or a silicon nitride film, which is an inorganic substance, made it possible to fabricate a liquid crystal display device with even higher reliability.

Furthermore, by using such a TFT array substrate as to have a metal electrode film formed in place of the transparent conductive film, it was possible to fabricate a reflective liquid crystal display device.

<u>Example 2-3</u>

In a manner similar to that described in Example 2-1, a transparent glass substrate 201 that had been thoroughly cleaned was prepared, and a

silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy film, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer 204, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film layer 205 not containing impurities and an amorphous silicon (n+a-Si) film layer 206 containing an n-type impurity to 200 nm and 50 nm, respectively.

It should be noted that in this example a contact metal film is not deposited on the n+a-Si film layer 206, which is different from the foregoing Example 2-1.

Next, a first resist pattern 208 for the first photolithography was formed by a conventional method (Figs. 14(a) and 14(b)).

Thereafter, the n+a-Si film layer 206, the i-type a-Si film layer 205, the gate insulating film layer 204 (SiN_x film), and the G-S metal film layer 203 (Al-Ta film) were sequentially etched, thereby forming a first pattern 240 including a gate electrode 203' or a gate wiring line 203", a source segmented wiring line 209', a gate insulating film 204', and a semiconductor film (205'+206') which were stacked (Figs. 15(a) and 15(b)).

Then, the gate electrode 203' and the gate wiring line 203" were anodically oxidized in an electrolyte to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the gate electrode and the side surfaces of the gate wiring line (Figs. 16(a) and 16(b)). Thereafter, a

contact electrode metal film (Ti) 241 and a metal electrode film 242 composed of an aluminum film (Al) were vapor deposited by sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact electrode metal film and the metal electrode film were to be connected to pixel metal electrodes connected to drain regions and were to connect together segments of each source segmented wiring line connected to source regions (Figs. 17(a) and 17(b)).

Subsequently, a second resist pattern 208' for the second photolithography was formed by a conventional method (Figs. 18(a) and 18(b)). Then, part of the metal electrode film 242, the contact electrode metal film (Ti) 241, and the n+a-Si film 206' on the gate electrode were sequentially etched away, and the source segmented wiring line 209' was connected to a source region 213 by a portion of a contact electrode metal film (Ti) 241' and a metal electrode film pattern 242', and a pixel metal electrode film 243 was connected to a drain region 216 (Figs. 19(a) and 19(b)). At this point, segments of the source segmented wiring line 209', which had been previously severed and disconnected, were connected together on the gate wiring line 203" by the portion of the contact electrode metal film (Ti) 241' and the metal electrode film pattern 242' (Fig. 19(b)).

Finally, by using printing and baking a passivation film 217 of 300 nm was formed on the substrate, except for the periphery thereof, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal, which are to be connected to driving circuitry, were etched away, thus producing a TFT array substrate 245 having reflective pixel metal electrodes in the pixel

portions (Figs. 20(a) and 20(b)).

According to the present example, segments of each source segmented wiring line are connected together by the two layers of the contact metal electrode and the metal electrode, and therefore the resistance of the source segmented wiring lines was made extremely low.

In addition, by using aluminum or an aluminum-based alloy (such as an Al–Zr or Ag–Pd–Cu alloy) for the reflective pixel metal electrode, it was possible to fabricate a TFT array substrate with excellent reflectivity.

Moreover, by vapor depositing the silica-based undercoat film between the surface of the insulating substrate and the gate wiring line metal film by a sol-gel method, it was possible to absorb substrate deformation.

Forming the aluminum-based alloy film for the gate wiring line metal film made it possible to fabricate a TFT array substrate having few irregularities on the surface of the wiring lines.

In the step of oxidation, by carrying out anodic oxidation in a neutral solution, it was possible to fabricate a TFT array substrate having good gate insulating properties.

Here, when the oxide films of the side surfaces of the gate electrodes were neutral, anodic oxide films, it was possible to fabricate a TFT array substrate with high reliability.

In addition, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the gate insulating film, the semiconductor film, the contact electrode metal film, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring lines.

Forming the silicon nitride-based gate insulating film and the semiconductor film between the gate electrode metal and the contact metal electrode made it possible to fabricate a TFT array substrate having excellent stability.

When segments of each source segmented wiring line, which had been severed by the gate wiring lines, were interconnected together on the gate wiring lines by the two layers of the contact metal electrode and the metal electrode, it was possible to minimize level differences on the surface of the TFT array substrate.

Further, when part of the semiconductor film had a two-layered structure composed of an i-type layer and an n+-type layer, it was possible to reduce the contact resistance of the source and the drain.

Furthermore, when the undercoat film was formed between the surface of the insulating substrate and the gate wiring line metal film, it was possible to fabricate a TFT array substrate with high reliability.

Example 2-4

The actual fabrication process of a liquid crystal display device using the TFT array substrate obtained in Example 2-3 is described with reference to Fig. 21.

First, there were provided a TFT array substrate, similar to that of Example 2-3, fabricated using two masks, more specifically, a first TFT array substrate 323 including a first electrode group 321 arranged in a matrix and a transistor group 322 that drives the first electrodes; and a color filter substrate 326 including a second electrode 325 and a color filter

group 324 placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 327.

Next, the first and second substrates 323 and 326 were arranged such that their respective electrodes oppose one another, thus producing a cell having a gap of about 5 microns created by spacers 328 and adhesives 329. A TN liquid crystal 330 was then injected between the first and second substrates, and a polarizer 331 was arranged on the cell surface of the color filter side, thus completing a reflective liquid crystal display device.

Such a device was capable of displaying images in the direction of the arrow A, by driving each transistor using video signals.

<u>Example 2-5</u>

In a manner similar to that described in Example 2-1, a transparent glass substrate 201 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer 204, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film layer 205 not containing impurities and an amorphous silicon (n+a-Si) film layer 206 containing an n-type impurity to 50 nm and 50 nm,

respectively. Finally, a Ti metal film, serving as a contact metal film layer 207, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Then, the Ti metal film 207, the n+a-Si film layer 206, the i-type a-Si film layer 205, the gate insulating film layer (SiN_x film) 204, and the G-S metal film layer (Al–Zr film) 203 were sequentially etched, thereby forming a first pattern including a gate electrode 203' or a gate wiring line 203", a source segmented wiring line 209', a gate insulating film layer 204', and a semiconductor film (205'), which were stacked, and a first comb-shaped pixel metal electrode 251.

Next, the gate electrode 203', the gate wiring line 203", and the first comb-shaped pixel metal electrode 251 were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a metal (Al) electrode film was vapor deposited by sputtering to a film thickness of about 100 nm. The metal electrode film was to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and was to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography was formed by a conventional method. Then, part of the metal electrode film 212', the contact electrode 207', and the n+a-Si film 206' on the gate

electrode were sequentially etched away through to the i-type a-Si film, and the source segmented wiring line 209' was connected to a source region 213 by a portion of the contact electrode 7 and a metal electrode 214', and a second comb-shaped pixel metal electrode 252 was connected to a drain region 216 by a portion of the contact electrode metal 207'.

At this point, the source segmented wiring lines 209" and 209"', which had been previously severed, were connected together on the gate wiring line 203" by the metal electrode film pattern 214' via a portion of the contact electrode metal 7'.

Finally, by using printing and baking a silica passivation film 217 of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the i-type a-Si film 205 and the SiN_x film 204 on the gate electrode metal, which are to be connected to external driving circuitry, were etched away, thus producing a TFT array substrate 253 applicable to in-plane switching (IPS) mode liquid crystal display devices (Figs. 22(a) and 22(b)).

Here, by simultaneously etching portions that are to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes, it was possible to fabricate a TFT array substrate for the IPS mode device, without additional masks.

In addition, carrying out the step of forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to fabricate a TFT array substrate having excellent stability.

Moreover, by sequentially forming the gate wiring line metal film, the

gate insulating film, and the semiconductor film, it was possible to prevent contamination of the channel portions.

In the oxidation step, carrying out anodic oxidation in a neutral electrolyte made it possible to selectively oxidize and insulate only the side surfaces of the gate electrodes and the side surfaces of the first comb-shaped pixel electrodes.

When the first comb-shaped pixel electrodes and part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the semiconductor film, the contact electrode metal film, and the metal electrode film, it was possible to provide a TFT array substrate having little resistance of the source segmented wiring line.

Further, when the contact electrode metal was formed for connecting the semiconductor films and the comb-shaped electrodes, it was possible to provide a TFT array substrate having low drain contact resistance.

When segments of each source segmented wiring line, which had been severed by the gate wiring lines and the first comb-shaped electrodes, were interconnected together on the gate wiring lines and the first comb-shaped electrodes by the contact electrode metal and the metal electrode, it was possible to provide a TFT array substrate having few level differences on the surface.

Moreover, when part of the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer, it was possible to provide a TFT array substrate having even lower contact resistance.

By forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film, it was possible to prevent

impurities migrating from the substrate from diffusing, providing a TFT array substrate with high reliability.

Example 2-6

The actual fabrication process of an IPS mode liquid crystal display device using the above-described TFT array substrate is described.

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-5, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group arranged in a matrix and a transistor group that drives the first electrodes; and a color filter substrate including a color filter group placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 5 microns created by spacers and adhesives. Thereafter, a nematic liquid crystal was injected between the first and second substrates, and polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device. (Drawings of the present example are similar to those in Figs. 19(a) and 19(b) except that a second electrode 225 is absent in the present example, and thus are omitted.)

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the

backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

At this point, after the step of fabricating TFT array substrate for the IPS mode device prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film, it was possible to fabricate a liquid crystal display device with high reliability.

Here, after the step of fabricating the bottom-gate TFT array substrate prior to the formation of the alignment films, by covering at least part of the TFT array substrate by a passivation film and etching, with use of this passivation film as a mask, the metal electrode film, the contact electrode metal film, the semiconductor film, and the gate insulating film to expose gate wiring line terminals, it was possible to fabricate a liquid crystal display device at low cost.

In addition, for the passivation film, forming a film composed of an inorganic substance such as a silica film or a silicon nitride film made it possible to fabricate a liquid crystal display device with excellent reliability.

<u>Example 2-7</u>

In a manner similar to that described in Example 2-3, a transparent glass substrate 201 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film

thickness of about 200 nm. Subsequently, a SiN_x film 4, serving as a gate insulating film, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film 205 not containing impurities and an amorphous silicon (n+a-Si) film 206 containing an n-type impurity to 200 nm and 50 nm, respectively. Then, a first resist pattern 208 for the first photolithography, which includes first comb-shaped pixel electrodes, was formed by a conventional method.

Thereafter, the n+a-Si film 206, the i-type a-Si film 205, the SiN_x film 204, and the Al-Ta film 203 were sequentially etched, thereby forming a first pattern including a gate electrode 203' or a gate wiring line 203", a source segmented wiring line 209', a gate insulating film layer 204', and a semiconductor film (205'), which were stacked, and a first comb-shaped pixel electrode 261.

Next, the gate electrode 203', the gate wiring line 203", and the first comb-shaped pixel electrode 261 were anodically oxidized in an electrolyte of ammonium borate to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a contact electrode metal (Ti) film 241 and a metal electrode film 242 composed of an aluminum film (Al) were vapor deposited by sputtering to film thicknesses of about 50 nm and 100 nm, respectively. The contact electrode metal film and the metal electrode film were to be connected to source regions and to second comb-shaped pixel metal electrodes connected to drain regions and were to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography,

which includes second comb-shaped pixel metal electrodes, was formed by a conventional method. Then, part of the metal electrode film 242, the contact electrode metal (Ti) 41, and the n+a-Si film 206' on the gate electrode were sequentially etched away, and the source segmented wiring line 209' was connected to a source region 213 by a portion of a contact electrode metal (Ti) film 241' and a metal electrode film pattern 242', and a second comb-shaped pixel metal electrode 262 was connected to a drain region 216 by a portion of the contact metal electrode.

At this point, segments of the source segmented wiring line 209', which had been previously severed, were connected together on the gate wiring line 203" by the portion of the contact electrode metal (Ti) film pattern 241' and the metal electrode film pattern 242'.

Finally, by using printing and baking a passivation film 217 of 300 nm was formed so as to cover the TFTs, and subsequently using this silica passivation film pattern as a mask, portions of the oxide film on the gate electrode metal which were to be connected to driving circuitry were etched away, thus producing a TFT array substrate 263 having the second comb-shaped pixel metal electrodes in the pixel portions (Figs. 23(a) and 23(b)).

Here, when the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer and part of the n-type layer was etched to the i-type layer, it was possible to fabricate a TFT array substrate at low cost without additional masks.

Further, by forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film, it was possible to

prevent impurities generating from the substrate from diffusing, allowing fabrication of a TFT array substrate with high reliability.

When the gate wiring line metal film, the gate insulating film, and the semiconductor film were sequentially formed, contamination of the channel portions was kept to a minimum, allowing fabrication of a TFT array substrate having stable Vt.

In the step of oxidation, by carrying out anodic oxidation in a neutral solution, it was possible to fabricate a TFT array substrate having few pinholes and little leakage current.

Moreover, when part of the TFT array substrate was covered, using a sol-gel method, by a passivation film composed of silica or a silica-containing inorganic substance, it was possible to fabricate a TFT array substrate with high reliability.

Example 2-8

The actual fabrication process of a liquid crystal display device using the above-described TFT array substrate is described.

First, there were provided a TFT array substrate for the IPS mode device, similar to that of Example 2-7, fabricated using two masks, more specifically, a first TFT array substrate including a first comb-shaped electrode group arranged in a matrix and a transistor group that drives the first electrodes; and a color filter substrate including a color filter group placed opposite to the first electrode group. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal

alignment films.

Next, the first and second substrates were arranged such that their respective alignment films oppose one another, thus producing a cell having a gap of about 4 microns created by spacers and adhesives. In addition, a nematic liquid crystal was injected between the first and second substrates, and two polarizers were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

Furthermore, when the metal electrode and the contact metal electrode were formed in a single layer with the same material, it was possible to further simplify the process.

Example 2-9

In a manner similar to that described in Example 2-1, a transparent glass substrate 1 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source

segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer 204, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film 205 not containing impurities and an amorphous silicon (n+a-Si) film 206 containing an n-type impurity to 50 nm and 50 nm, respectively. Finally, a Ti metal film, serving as a contact metal film layer 207, was vapor deposited by sputtering to a film thickness of about 100 nm. Thereafter, a first resist pattern 208 for the first photolithography was formed by a conventional method.

Then, the Ti metal film 207, the n+a-Si film 206, the i-type a-Si film 205, the SiN_x film 204, and the Al–Zr film 203 were sequentially etched, thereby forming a first pattern 210 including a gate electrode 203' or a gate wiring line 203", a source segmented wiring line 209', a gate insulating film layer 204', a semiconductor film (205' and 206'), and a contact electrode metal 207' which were stacked.

Next, the gate electrode 3' and the gate wiring line 3" were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a metal electrode film was vapor deposited by sputtering to a film thickness of about 100 nm. The metal electrode film was to be connected to source regions and to first comb-shaped pixel metal electrodes connected to drain regions and was to connect together segments of each severed source segmented wiring line.

Subsequently, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a conventional method. Then, part of the transparent conductive film 212, the contact electrode 207', and the n+a-Si film 206' on the gate electrode were sequentially etched away through to the i-type a-Si film, and the source segmented wiring line 209' was connected to a source region 213 by a portion of the contact electrode 207' and a metal electrode 214", and the first comb-shaped pixel metal electrode 71 was connected to a drain region 216 by a portion of the contact electrode metal 207'.

At this point, the source segmented wiring lines 209" and 209"', which had been previously severed, were connected together on the gate wiring line 203" by the metal electrode 214" via a portion of the contact electrode metal 207'.

Subsequently, a silica passivation film 217 of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film 205 and the SiN_x film 204 on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

An Al–Zr alloy was then vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode 272 was formed, thus producing a TFT array substrate 273 applicable to IPS mode transmissive liquid crystal display devices, with the use of three photomasks (Figs. 24(a) and 24(b)).

Here, when the semiconductor film had a two-layered structure

composed of an i-type layer and an n-type layer and part of the n-type layer was etched to the i-type layer, it was possible to simplify the TFT process.

In addition, forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to fabricate a TFT array substrate having stable characteristics.

When at least the gate wiring line metal film, the gate insulating film, and the semiconductor film were sequentially formed, it was possible to prevent contamination of the channel interfaces.

In the step of oxidation, by carrying out anodic oxidation, it was possible to form an insulating film having few pinholes, allowing fabrication of a TFT array substrate having little gate leakage.

Here, when the oxide films of the side surfaces of the gate electrodes were formed of anodic oxide films, it was possible to fabricate a TFT array substrate having excellent leakage characteristics.

Furthermore, when part of the source segmented wiring line had a five-layered structure composed of the gate wiring line metal film, the semiconductor film, the contact electrode metal film, and the metal electrode film, it was possible to reduce the resistance of the source segmented wiring line, allowing fabrication of a TFT array substrate having few variations in characteristics.

When a contact electrode metal was formed between the semiconductor film and the source/drain electrodes, it was possible to fabricate a TFT array substrate having little internal resistance.

Moreover, when segments of each source segmented wiring line, which had been severed by the gate wiring lines, were interconnected together on

the gate wiring lines by the contact electrode metal and the metal electrode, it was possible to fabricate a TFT array substrate having a low resistance of the source segmented wiring line.

When part of the semiconductor film had a two-layered structure composed of an i-type layer and an n-type layer, it was possible to omit the step of diffusing an n-type impurity.

Forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film made it possible to minimize the influence of the substrate deformation.

Example 2-10

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-9 is described.

First, there were provided a TFT array substrate, similar to that of Example 2-9, fabricated using two masks, more specifically, a first TFT array substrate 223 including a first electrode group 221 arranged in a matrix and a transistor group 22 that drives the first electrodes; and a color filter substrate 226 including a color filter group 224 placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 227.

Next, the first and second substrates 223 and 226 were arranged such that the electrodes oppose one another, thus producing a cell having an alignment direction twisted 90 degrees and a gap of about 5 microns, which

is created by spacers 228 and adhesives 229. Thereafter, a TN liquid crystal 230 was injected between the first and second substrates, and polarizers 231 and 232 were then arranged so as to have a crossed Nicols relation, thus completing a display device. (A drawing of the present example is similar to that in Fig. 21 and thus is omitted.)

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 210.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability.

Example 2-11

In a manner similar to that described in Example 2-8, a transparent glass substrate 1 that had been thoroughly cleaned in advance was prepared, and a silica (SiO_2) film, serving as an undercoat film layer 202, was deposited by CVD to 0.4 microns. Then, an Al–Zr (97:3) alloy, serving as a G-S metal film layer 203 for gate electrodes, gate wiring lines, and source segmented wiring lines, was vapor deposited by sputtering to a film thickness of about 200 nm. Subsequently, a SiN_x film, serving as a gate insulating film layer 4, was deposited by plasma enhanced CVD to 150 nm, followed by, as a semiconductor film, an amorphous silicon (i-type a-Si) film 205 not containing impurities and an amorphous silicon (n+a-Si) film 206

containing an n-type impurity to 50 nm and 50 nm, respectively, and then a first resist pattern 208 for the first photolithography was formed by a conventional method.

Thereafter, the n+a-Si film 206, the i-type a-Si film 205, the SiN_x film 204, and the Al–Zr film 203 were sequentially etched, thereby forming a first pattern 210 including a gate electrode 203' or a gate wiring line 203", a source segmented wiring line 209', a gate insulating film layer 204', and a semiconductor film (205' and 206') which were stacked.

Next, the gate electrode 203' and the gate wiring line 203" were anodically oxidized in an electrolyte using ammonium borate and having a pH in the neighborhood of 7, to form insulating films 211, mainly composed of Al_2O_3, on the side surfaces of the pattern.

Further, a Ti metal film, serving as a contact metal film layer 207, was vapor deposited by sputtering to a film thickness of about 100 nm, and subsequently an Al–Zr film, serving as a metal electrode film, was vapor deposited by sputtering to a film thickness of about 100 nm. The contact metal film layer and the metal electrode film are to be connected to source regions and to first comb-shaped pixel metal electrodes connected to drain regions, and to connect together segments of each severed source segmented wiring line.

Thereafter, a second resist pattern for the second photolithography, which includes a first comb-shaped electrode pattern, was formed by a conventional method. Subsequently, part of the transparent conductive film 12, the contact electrode 7', and the n+a-Si film 6' on the gate electrode were sequentially etched away through to the i-type a-Si film, and the

source segmented wiring line 209' was connected to a source region 13 by a portion of the contact electrode 207' and a metal electrode 14", and the first comb-shaped pixel metal electrode 81 was connected to a drain region 16 by a portion of the contact electrode metal 7'.

At this point, the source segmented wiring lines 9" and 9"', which had been previously severed, were connected together on the gate wiring line 3" by the two-layered structure composed of the metal electrode 14" and a portion of the contact electrode metal 7'.

Subsequently, a silica passivation film 17 of 300 nm was formed by printing and baking, using a sol-gel method, so as to cover the TFTs. Thereafter, using this silica passivation film pattern as a mask, portions of the i-type a-Si film 5 and the SiN_x film 4 on the gate electrode metal, which are to be connected to external driving circuitry, were etched away.

Finally, an Al–Zr alloy was once again vapor deposited on the entire surface to a film thickness of 150 nm, and using a photomask having a second comb-shaped electrode pattern, a second comb-shaped pixel metal electrode 82 was formed, thus producing a TFT array substrate 83 applicable to IPS mode transmissive liquid crystal display devices, with the use of three photomasks (Figs. 25(a) and 25(b)).

Consequently, because at least segments of each source segmented wiring line were connected together by the two-layered structure composed of the metal electrode and the contact electrode metal, it was possible to reduce the resistance of the source segmented wiring line, allowing fabrication of a TFT array substrate having excellent image display characteristics.

Example 2-12

The actual fabrication process of a liquid crystal display device using the TFT array substrate produced in the foregoing Example 2-11 is described.

First, there were provided a TFT array substrate, similar to that of Example 2-9, fabricated using two masks, more specifically, a first TFT array substrate 223 including a first electrode group 221 arranged in a matrix and a transistor group 222 that drives the first electrodes; and a color filter substrate 226 including a color filter group 224 placed opposite to the first and second comb-shaped electrode groups. Over each of the substrates, by a conventional method, a polyimide resin was applied and cured, and the resulting films were subjected to rubbing, thus producing liquid crystal alignment films 227.

Next, the first and second substrates 223 and 226 were arranged such that the electrodes oppose one another, thus producing a cell having an alignment direction twisted 90 degrees and a gap of about 5 microns, which is created by spacers 228 and adhesives 229. Thereafter, a TN liquid crystal 230 was injected between the first and second substrates, and polarizers 231 and 232 were then arranged so as to have a crossed Nicols relation, thus completing a display device.

Such a device was capable of displaying images by driving each transistor using video signals while lighting, using the backlight from the backside. Here, the device achieved a wide viewing angle of 160° horizontally and vertically with a contrast of 10.

Here, after the step of fabricating the TFT array substrate prior to the formation of the alignment films, by carrying out the step of covering at least part of the TFT array substrate by a passivation film such as silica, it was possible to fabricate a liquid crystal display device with high reliability. (A drawing of the present example is similar to that in Fig. 21 and thus is omitted.)

INDUSTRIAL APPLICABILITY

As has been explained above, according to the present invention, it is possible to fabricate an electrical circuit board having X-Y wiring lines that intersect one another in the plane, with extremely high productivity. Such an electrical circuit board is applicable in a wide range of electronic device applications. In addition, the TFT array substrates in accordance with the present invention, to which such an electrical circuit board is applied, can be fabricated with the use of two photomasks, and therefore a substantial reduction in the fabrication costs of TFT array substrates is achieved. Moreover, using such TFT array substrates produces the advantageous effect of providing liquid crystal display devices at a lower cost. Thus, the value of the present invention to industry is considerable.

What is claimed is:

1. An electrical circuit board comprising:

X wiring lines and Y segmented wiring lines, each of the wiring lines being formed of a same conductive metal film and in a same plane on an insulating substrate and the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines;

wherein top and side surfaces of the X wiring lines are covered with an insulating film; and

segments of each of the Y segmented wiring lines are electrically connected together by a Y segmented wiring line-connecting electrode formed on the insulating film.

2. The electrical circuit board according to claim 1, wherein the insulating film of at least the side surfaces of the X wiring lines is a metal oxide film formed by oxidizing the conductive metal film.

3. The electrical circuit board according to claim 2, wherein the metal oxide film is an anodic oxide film formed by anodic oxidation.

4. A method of fabricating an electrical circuit board comprising:

a first step of depositing a conductive metal film layer over an insulating substrate;

a second step of etching the conductive metal film layer to

simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being distanced from the X wiring lines;

a third step, after the second step, of oxidizing top and side surfaces of the X wiring lines to cover the top and side surfaces by an insulating metal oxide film; and

a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

5. The method of fabricating an electrical circuit board according to claim 4, wherein the third step of oxidizing the X wiring lines is carried out by anodic oxidation.

6. A method of fabricating an electrical circuit board comprising:

a first step of sequentially depositing at least a conductive metal film layer and an insulating film layer over an insulating substrate;

a second step of etching layers including the insulating film layer and the conductive metal film layer to simultaneously form X wiring lines and Y segmented wiring lines in a same plane, the Y segmented wiring lines intersecting with the X wiring lines, being severed by the X wiring lines at the intersections, and being

distanced from the X wiring lines;

a third step, after the second step, of oxidizing side surfaces of the X wiring lines to cover the side surfaces by an insulating metal oxide film; and

a fourth step, after the third step, of depositing a conductive film layer so as to cover at least the intersections, whereby segments of each of the Y segmented wiring lines are electrically connected together, each of the Y segmented wiring lines being severed by and distanced from the X wiring lines.

7. The method of fabricating an electrical circuit board according to claim 6, wherein the third step of oxidizing the side surfaces of the X wiring lines is carried out by anodic oxidation.

8. A bottom-gate TFT array substrate comprising:

gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film;

a gate insulating film stacked on each of the gate electrodes;

a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions;

source contact electrodes stacked on the source regions of the semiconductor film;

drain contact electrodes stacked on the drain regions of the semiconductor film;

pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes;

gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film;

source segmented wiring lines formed in a same plane as the gate wiring lines, each of the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and

source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines.

9. The bottom-gate TFT array substrate according to claim 8, wherein the pixel electrodes and the source wiring line-connecting electrodes are composed of a same transparent conductive film material.

10. The bottom-gate TFT array substrate according to claim 9 wherein:

a source segmented wiring line section pattern has a five-layered structure composed of the source segmented wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the source segmented wiring lines are located at the bottom of the five-layered structure;

a gate wiring line section pattern has a five-layered structure composed of the gate wiring lines, a gate insulating film, a semiconductor film, a contact metal film, and a transparent conductive film, and the gate wiring lines are located at the bottom of the five-layered structure; and

the source segmented wiring lines and the gate wiring lines are in the same plane on the substrate.

11. The bottom-gate TFT array substrate according to claim 10, wherein the insulating film of at least the side surfaces of the gate wiring lines is composed of an oxide film formed from the conductive metal film.

12. The bottom-gate TFT array substrate according to claim 11, wherein the oxide film is an anodic oxide film formed by anodic oxidation.

13. The bottom-gate TFT array substrate according to claim 11, wherein the semiconductor film has a two-layered structure composed of an i-type amorphous silicon layer and an n-type amorphous silicon layer.

14. The bottom-gate TFT array substrate according to claim 9, wherein in place of the transparent conductive film material, a light reflective conductive film material is used.

15. A method of fabricating a bottom-gate TFT array substrate comprising:

(A) sequentially depositing at least a G-S metal film layer, a gate

insulating film layer, a semiconductor film layer, and a contact metal film layer over a surface of an insulating substrate, the G-S metal film layer to be formed into gate electrodes, gate wiring lines, and source segmented wiring lines;

(B), after step (A), by photolithography, using a first resist pattern, etching the layers through to the surface of the insulating substrate to form a gate electrode section pattern, a gate wiring line section pattern, and a source segmented wiring line section pattern, the gate electrode section pattern including gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate electrodes, the gate wiring line section pattern including gate wiring lines connected to the gate electrodes and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the gate wiring lines, and the source segmented wiring line section pattern including source segmented wiring lines, which are severed and distanced at the intersections of the source segmented wiring lines and the gate wiring lines, and the gate metal film, the gate insulating film, the semiconductor film, and the contact metal film which are sequentially stacked on the source segmented wiring lines;

(C), after step (B), etching the contact metal film of the gate electrode section pattern through to a surface of the semiconductor film to form on the semiconductor film, and oxidizing side surfaces of the

gate electrodes and side surfaces of the gate wiring lines to form an electrically insulating metal oxide film;

(E), after step (C), depositing a transparent conductive film layer on top of the contact metal film over the entire surface of the substrate so that at least segments of each source segmented wiring line are electrically connected together by the conductive film; and

(F), after step (E), by photolithography, using a second resist pattern, etching the transparent conductive film layer in a predetermined pattern to form pixel electrodes and channel regions exposed by the etching.

16. The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein the oxidation of the side surfaces of the gate wiring lines is carried out by anodic oxidation.

17. The method of fabricating a bottom-gate TFT array substrate according to claim 15 wherein:

the semiconductor film layer has a two-layered structure composed of an n-type amorphous silicon layer and an i-type amorphous silicon layer; and

step (F) of etching the contact metal film of the gate electrode section pattern is carried out such that part of the contact metal film and part of the n-type amorphous silicon layer immediately below the contact metal film are etched through to the i-type amorphous

silicon layer.

18. The method of fabricating a bottom-gate TFT array substrate according to claim 15, wherein in place of the transparent conductive film layer in step (E), a light reflective conductive film layer is deposited.

19. A liquid crystal display device comprising;

a bottom-gate TFT array substrate including gate electrodes formed directly on a substrate or with an undercoat film layer disposed between the gate electrodes and the substrate, side surfaces of the gate electrodes being covered with an insulating film; a gate insulating film stacked on the gate electrodes; a semiconductor film stacked on the gate insulating film, the semiconductor film having source regions, drain regions, and channel regions between the source regions and the drain regions; source contact electrodes stacked on the source regions of the semiconductor film; drain contact electrodes stacked on the drain regions of the semiconductor film; pixel electrodes connected to the drain regions of the semiconductor film by the drain contact electrodes; gate wiring lines connected to the gate electrodes, top and side surfaces of the gate wiring lines being covered with an insulating film; source segmented wiring lines formed in a same plane as the gate wiring lines, the source segmented wiring lines intersecting with the gate wiring lines in the same plane and being severed by and distanced from the gate wiring lines at the intersections; and

source wiring line-connecting electrodes for electrically connecting segments of each source segmented wiring line together on the gate wiring lines; and

a counter substrate;

wherein the TFT array substrate and the counter substrate are opposed to each other with a surface on which the TFTs are being formed facing inside and with a predetermined gap therebetween, a liquid crystal being held in the gap.

20. The liquid crystal display device according to claim 19, wherein a surface of the TFT array substrate is protected by a passivation film.

21. The liquid crystal display device according to claim 20, wherein the passivation film is one selected from the group consisting of a silica film and a silicon nitride film.

22. The liquid crystal display device according to claim 19, wherein the pixel electrodes are composed of a transparent metal film.

23. The liquid crystal display device according to claim 19, wherein the pixel electrodes are composed of a light reflective metal film.

24. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a reflective pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the reflective pixel metal electrodes has a two-layered structure composed of a contact metal electrode and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact metal electrode; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode.

25. The bottom-gate TFT array substrate according to claim 24, wherein the reflective pixel metal electrode group is one selected from the group consisting of aluminum and an aluminum-based alloy.

26. The bottom-gate TFT array substrate according to claim 24, wherein part of each source segmented wiring line has a two-layered structure composed of a contact electrode metal film and an aluminum-based metal electrode film.

27. The bottom-gate TFT array substrate according to claim 24, wherein the gate insulating film and the semiconductor film are formed between the gate electrode metal and the contact metal electrode.

28. The bottom-gate TFT array substrate according to claim 24, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected

together on the gate wiring lines by the two layers of the contact metal electrode and the metal electrode.

29. The bottom-gate TFT array substrate according to claim 24, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n+-type layer.

30. The bottom-gate TFT array substrate according to claim 24, wherein an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

31. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact electrode metal film and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

32. The method of fabricating a bottom-gate TFT array substrate

according to claim 31, wherein the metal electrode film is an aluminum or aluminum-based alloy film.

33. The method of fabricating a bottom-gate TFT array substrate according to claim 31, further comprising forming a silica-based undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

34. The method of fabricating a bottom-gate TFT array substrate according to claim 31, wherein at least an aluminum-based alloy film is formed for the gate wiring line metal film.

35. The method of fabricating a bottom-gate TFT array substrate according to claim 31, wherein the oxidation is carried out, by anodic oxidation, in a neutral solution.

36. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; reflective pixel metal electrodes each having a two-layered structure composed of a contact metal electrode and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact metal electrode; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact metal electrode

and a metal electrode; and

a color filter substrate having a color filter side on which a counter transparent electrode is formed;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

37. The liquid crystal display device according to claim 36, wherein at least part of the TFT array is covered with a passivation film.

38. The liquid crystal display device according to claim 37, wherein the passivation film is an inorganic substance.

39. A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; and by photolithography, etching part of the

metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a counter electrode side of a color filter substrate having a counter transparent electrode formed thereon;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

40. The method of fabricating a liquid crystal display device according to claim 39, further comprising, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film.

41. The method of fabricating a liquid crystal display device according to claim 39, wherein the metal electrode and the contact metal electrode are formed in a single layer with a same material.

42. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes, side surfaces of the gate wiring lines, and side surfaces of the first comb-shaped pixel electrodes are oxidized;

each of the second comb-shaped pixel metal electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode.

43. The bottom-gate TFT array substrate according to claim 42, wherein the oxide film of the side surfaces of the gate electrodes and of the first comb-shaped pixel electrodes is an anodic oxide film.

44. The bottom-gate TFT array substrate according to claim 42, wherein the first comb-shaped pixel electrodes and part of each source segmented wiring line have a five-layered structure composed of a gate wiring line metal film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

45. The bottom-gate TFT array substrate according to claim 42, wherein the contact electrode metal is formed to connect each of the comb-shaped electrodes to the semiconductor film.

46. The bottom-gate TFT array substrate according to claim 42, wherein the source segmented wiring lines are severed by the gate wiring

lines and the first comb-shaped electrodes, and segments of each source segmented wiring line are interconnected together on the gate wiring lines and the first comb-shaped electrodes by a contact electrode metal and the metal electrode.

47. The bottom-gate TFT array substrate according to claim 42, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

48. The bottom-gate TFT array substrate according to claim 42, wherein an undercoat film is formed between a surface of the insulating substrate and a gate wiring line metal film.

49. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate;

by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes;

forming a metal electrode film; and

by photolithography, sequentially etching part of the metal electrode

film, the contact electrode metal film, and the semiconductor film, using a second pattern.

50. The method of fabricating a bottom-gate TFT array substrate according to claim 49, wherein portions to be formed into the gate wiring lines, the gate electrodes, and the first comb-shaped pixel electrodes are simultaneously etched.

51. The method of fabricating a bottom-gate TFT array substrate according to claim 49, further comprising forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

52. The method of fabricating a bottom-gate TFT array substrate according to claim 49, wherein at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

53. The method of fabricating a bottom-gate TFT array substrate according to claim 49, wherein the oxidation is carried out by anodic oxidation.

54. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes, gate wiring lines, and first comb-shaped electrodes, at least side surfaces of the gate electrodes, of the gate wiring lines, and of the first comb-shaped

electrodes being oxidized; second comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; and source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

55. The liquid crystal display device according to claim 54, wherein at least part of the TFT array is covered with a passivation film.

56. The liquid crystal display device according to claim 55, wherein the passivation film is an inorganic substance.

57. A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring

line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped pixel electrodes; forming a metal electrode film; and by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

58. The method of fabricating a liquid crystal display device according to claim 57, further comprising:

after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at least part of the TFT array by a passivation film; and

using the passivation film as a mask, etching the metal electrode film, the contact electrode metal film, the semiconductor film, and the gate insulating film, to expose gate wiring line terminals.

59. The method of fabricating a liquid crystal display device according to

to claim 58, wherein the passivation film is a silica film or a silicon nitride film.

60. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel metal electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the comb-shaped reflective pixel metal electrodes has a two-layered structure composed of a contact metal electrode and another metal electrode film and is connected to a drain region of a corresponding TFT by the contact metal electrode; and

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode.

61. The bottom-gate TFT array substrate according to claim 60, wherein an aluminum-based metal is used for the gate electrodes, and the insulating film of the side surfaces is an anodic oxide film.

62. The bottom-gate TFT array substrate according to claim 60, wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a gate insulating film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

63. The bottom-gate TFT array substrate according to claim 60, wherein the contact metal electrode is formed between a source electrode and the semiconductor film and between the comb-shaped electrode and the semiconductor film.

64. The bottom-gate TFT array substrate according to claim 60, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by the two layers of the contact metal electrode and the metal electrode.

65. The bottom-gate TFT array substrate according to claim 60, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

66. The bottom-gate TFT array substrate according to claim 60, wherein an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

67. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes;

forming a contact electrode metal film and a metal electrode film; and

by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern.

68. The method of fabricating a bottom-gate TFT array substrate according to claim 67, wherein the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched through to the i-type layer.

69. The method of fabricating a bottom-gate TFT array substrate according to claim 67, further comprising forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

70. The method of fabricating a bottom-gate TFT array substrate according to claim 67, wherein at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

71. The method of fabricating a bottom-gate TFT array substrate according to claim 67, wherein the oxidation is carried out by anodic oxidation.

72. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an array side, the array side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each having a two-layered structure composed of a contact metal electrode and another metal electrode film and being connected to a drain region of a corresponding TFT by the contact metal electrode; and source segmented wiring lines each connected to a source region of a corresponding TFT by two layers of a contact metal electrode and a metal electrode; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the array side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

73. The liquid crystal display device according to claim 72, wherein at least part of the TFT array is covered with a passivation film.

74. The liquid crystal display device according to claim 72, wherein the passivation film is an inorganic substance.

75. A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a gate wiring line metal film pattern to be formed into gate wiring lines, gate electrodes, and first comb-shaped electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a counter electrode side of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

76. The method of fabricating a liquid crystal display device according to claim 75, further comprising, after the fabrication of the bottom-gate TFT array substrate prior to the formation of the alignment films, covering at

least part of the TFT array by a passivation film.

77. The method of fabricating a liquid crystal display device according to claim 75, wherein the metal electrode and the contact metal electrode are formed in a single layer with a same material.

78. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel electrodes is connected to a drain region of a corresponding TFT by a contact electrode metal;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped opposing electrodes are formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

79. The bottom-gate TFT array substrate according to claim 78, wherein the oxide film of the side surfaces of the gate electrodes is an anodic oxide film.

80. The bottom-gate TFT array substrate according to claim 78,

wherein part of each source segmented wiring line has a five-layered structure composed of a gate wiring line metal film, a semiconductor film, a contact electrode metal film, and a metal electrode film.

81. The bottom-gate TFT array substrate according to claim 78, wherein the contact electrode metal is formed between the semiconductor film and a source electrode and between the semiconductor film and a drain electrode.

82. The bottom-gate TFT array substrate according to claim 78, wherein the source segmented wiring lines are severed by the gate wiring lines, and segments of each source segmented wiring line are interconnected together on the gate wiring lines by a contact electrode metal and the metal electrode.

83. The bottom-gate TFT array substrate according to claim 78, wherein part of the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer.

84. The bottom-gate TFT array substrate according to claim 78, wherein an undercoat film is formed between a surface of the insulating substrate and the gate wiring line metal film.

85. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, a

semiconductor film, and a contact electrode metal film on a surface of an insulating substrate;

by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and

forming second comb-shaped opposing electrodes using a third pattern with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

86. The method of fabricating a bottom-gate TFT array substrate according to claim 85, wherein the semiconductor film has a two-layered structure composed of an i-type layer and an n-type layer, and part of the n-type layer is etched.

87. The method of fabricating a bottom-gate TFT array substrate according to claim 85, further comprising forming an undercoat film between the surface of the insulating substrate and the gate wiring line metal film.

88. The method of fabricating a bottom-gate TFT array substrate

according to claim 85, wherein at least the gate wiring line metal film, the gate insulating film, and the semiconductor film are sequentially formed.

89. The method of fabricating a bottom-gate TFT array substrate according to claim 85, wherein the oxidation is carried out by anodic oxidation.

90. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel metal electrodes each connected to a drain region of a corresponding TFT by a contact electrode metal; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped opposing electrodes formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on

each of the substrates.

91. The liquid crystal display device according to claim 90, wherein at least part of the TFT array is covered with a passivation film.

92. The liquid crystal display device according to claim 91, wherein the passivation film is an inorganic substance.

93. A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film on a surface of an insulating substrate; by photolithography, sequentially etching the contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes, using a third pattern, with a passivation film disposed between the second comb-shaped opposing electrodes and the substrate;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a color filter side of a color

filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

94. The method of fabricating a liquid crystal display device according to claim 93, further comprising, after the formation of the second comb-shaped opposing electrodes, covering at least part of each second comb-shaped opposing electrode by a passivation film.

95. The method of fabricating a liquid crystal display device according to claim 93, wherein the passivation film is a silica film or a silicon nitride film.

96. A bottom-gate TFT array substrate comprising source segmented wiring lines, gate wiring lines, a gate insulating film, a semiconductor film, and a comb-shaped pixel electrode group, the bottom-gate TFT array substrate wherein:

at least side surfaces of gate electrodes and side surfaces of the gate wiring lines are oxidized;

each of the first comb-shaped pixel metal electrodes has a two-layered structure composed of a contact electrode metal and is connected to a drain region of a corresponding TFT;

each of the source segmented wiring lines is connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and

the second comb-shaped opposing electrodes are formed with an insulating film disposed between the second-comb shaped opposing electrodes and the substrate.

97. The bottom-gate TFT array substrate according to claim 96, wherein at least segments of each source segmented wiring line are connected together by a two-layered structure composed of the metal electrode and a contact electrode metal.

98. A method of fabricating a bottom-gate TFT array substrate comprising:

forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate;

by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern;

oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes;

forming a contact electrode metal film and a metal electrode film;

by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and

forming second comb-shaped opposing electrodes, using a third pattern, with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate.

99. A liquid crystal display device comprising:

a bottom-gate TFT array substrate having an electrode side, the electrode side including gate electrodes and gate wiring lines, at least side surfaces of the gate electrodes and side surfaces of the gate wiring lines being oxidized; first comb-shaped pixel electrodes each having a two-layered structure composed of a contact electrode metal and being connected to a drain region of a corresponding TFT; source segmented wiring lines each connected to a source region of a corresponding TFT by a contact electrode metal and a metal electrode; and second comb-shaped opposing electrodes formed with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate; and

a color filter substrate having a color filter side;

wherein the bottom-gate TFT array substrate and the color filter substrate are adhered together with the electrode side and the color filter side opposing to each other and with a predetermined gap maintained between the substrates, a liquid crystal being sandwiched in the gap and an alignment film being disposed on each of the substrates.

100. A method of fabricating a liquid crystal display device comprising:

fabricating a bottom-gate TFT array substrate including forming at least a gate wiring line metal film, a gate insulating film, and a semiconductor film on a surface of an insulating substrate; by photolithography, sequentially etching the semiconductor film, the gate insulating film, and the gate wiring line metal film, using a first pattern; oxidizing side surfaces of portions of a metal film pattern to be formed into gate wiring lines and gate electrodes; forming a contact electrode metal film and a metal electrode film; by photolithography, sequentially etching part of the metal electrode film, the contact electrode metal film, and the semiconductor film, using a second pattern; and forming second comb-shaped opposing electrodes, using a third pattern, with an insulating film disposed between the second comb-shaped opposing electrodes and the substrate;

forming an alignment film on the bottom-gate TFT array substrate;

forming an alignment film on a surface of a color filter side of a color filter substrate;

adhering and fixing the bottom-gate TFT array substrate and the color filter substrate at the periphery thereof such that the substrates are arranged with the two alignment films facing inside and with a predetermined gap maintained between the substrates; and

injecting a specified liquid crystal between the first and second substrates.

101. The method of fabricating a liquid crystal display device according

to claim 100, further comprising covering at least part of each second comb-shaped opposing electrode by a passivation film.

ABSTRACT

TFT array substrates used for liquid crystal display panels are disclosed of which the fabrication processes are simplified and the manufacturing costs are reduced by reducing the number of masks used in fabricating the TFT array substrates. A gate wiring line metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film are formed on a substrate surface. The contact electrode metal film, the semiconductor film, the gate insulating film, and the gate wiring line metal film are sequentially etched, by photolithography, using a first pattern, and the side surfaces of a gate wiring line metal film pattern, which is formed into portions of gate wiring lines and gate electrodes, are oxidized. A transparent conductive film is formed, and part of the transparent conductive film, the contact electrode metal film, and the semiconductor film are sequentially etched, by photolithography, using a second pattern.

Fig. 1

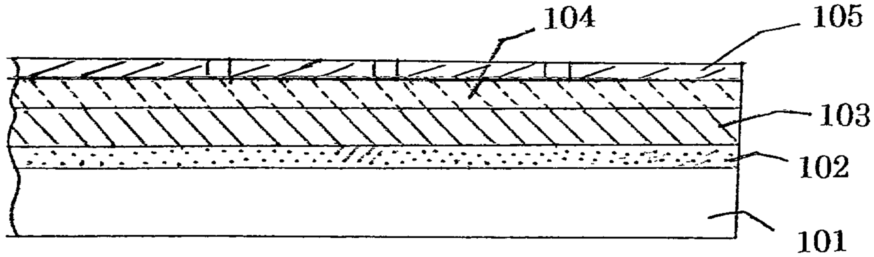

Fig. 2

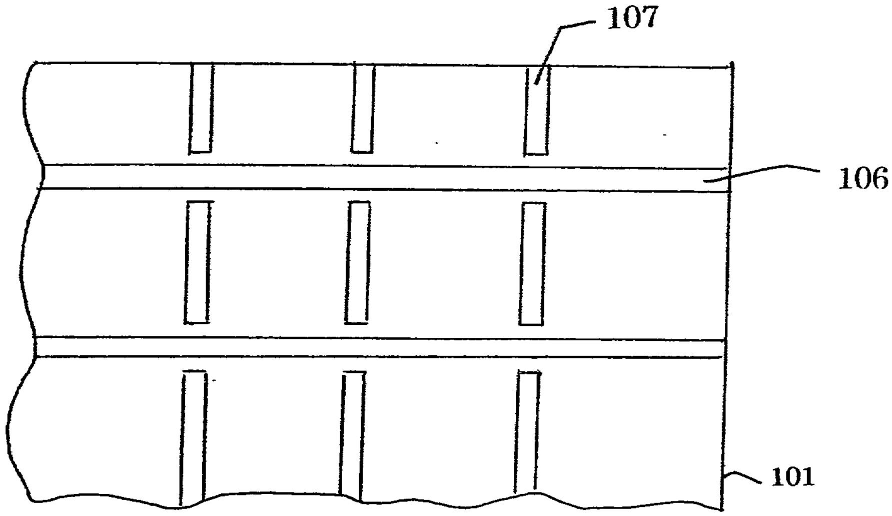

Fig. 3

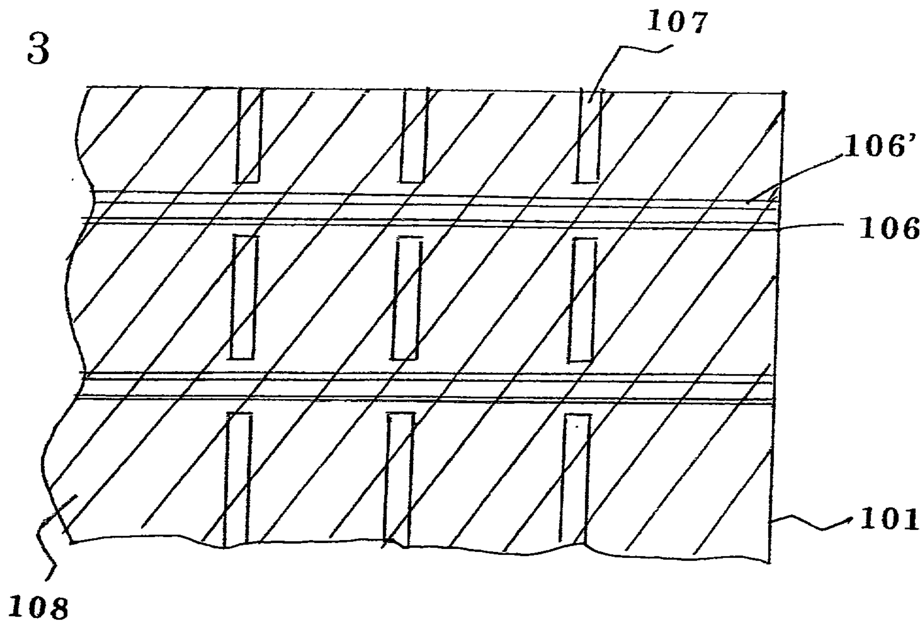

Fig. 4

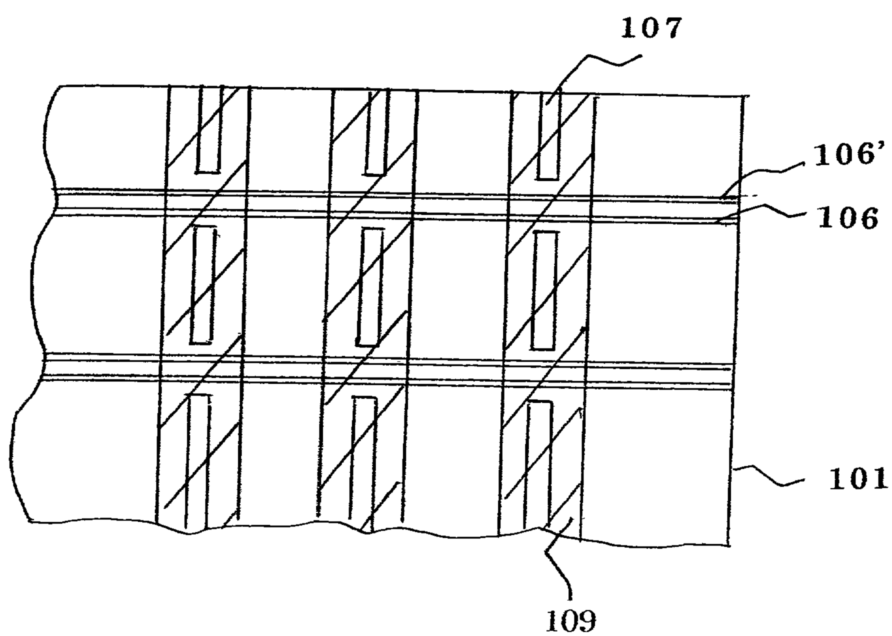

Fig. 5

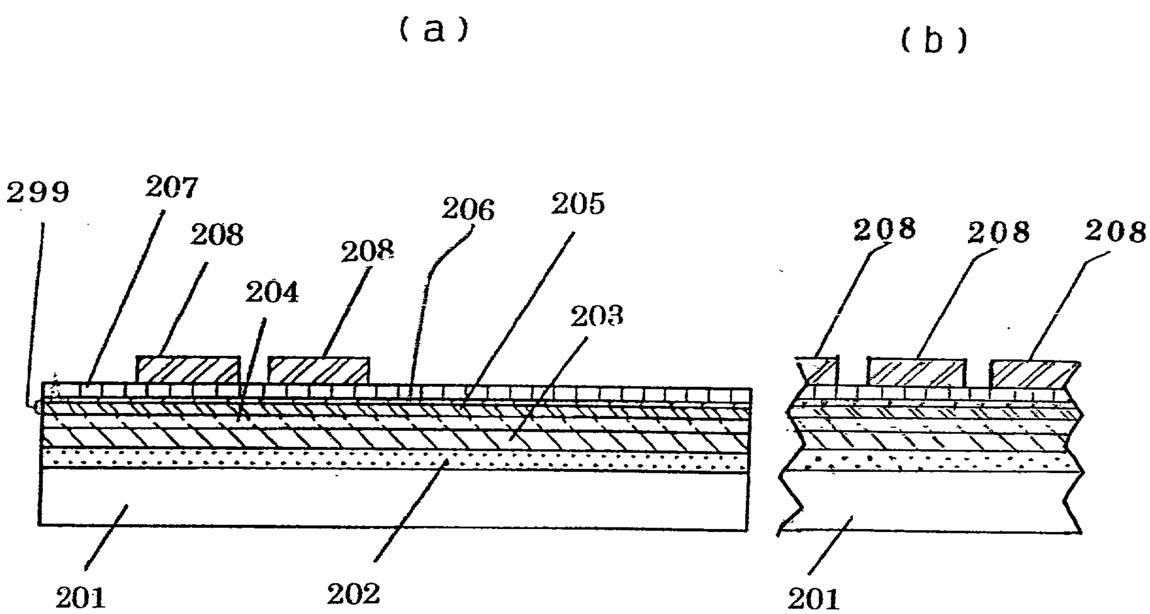
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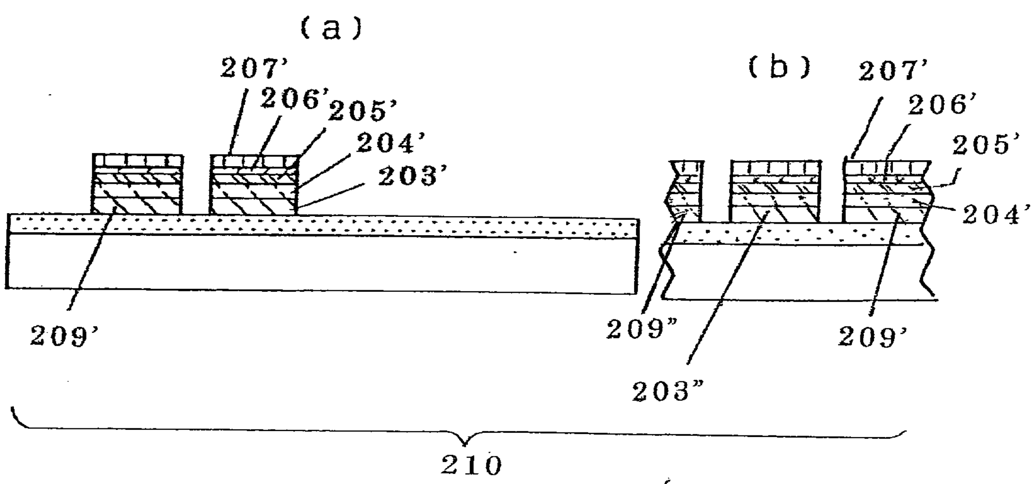
Fig. 6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(b)
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209'
203"
210

Fig. 7

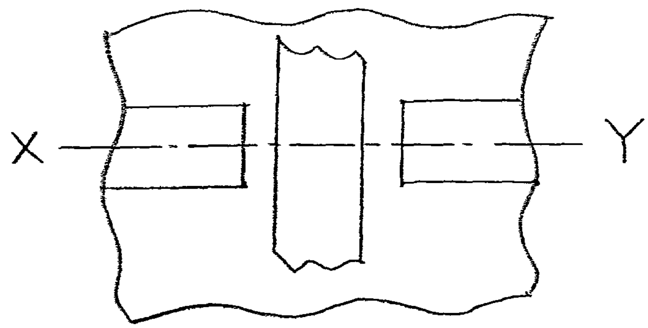

Fig. 8

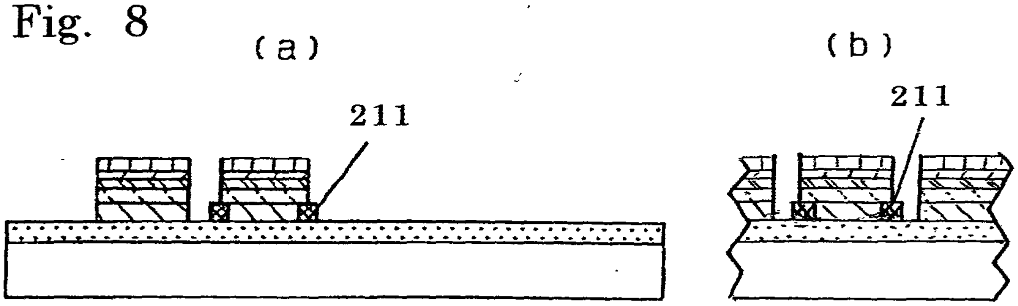

Fig. 9

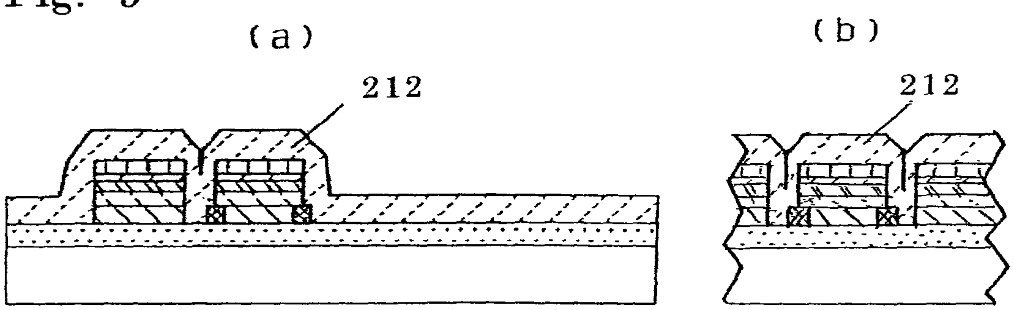

Fig. 10

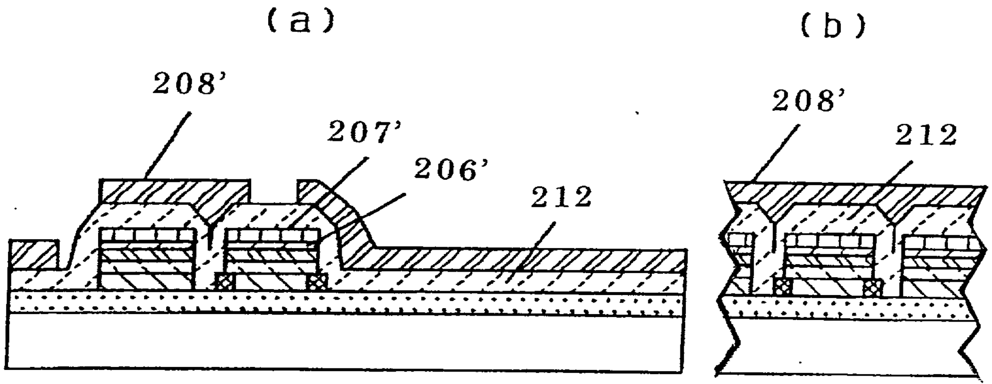
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Fig. 11

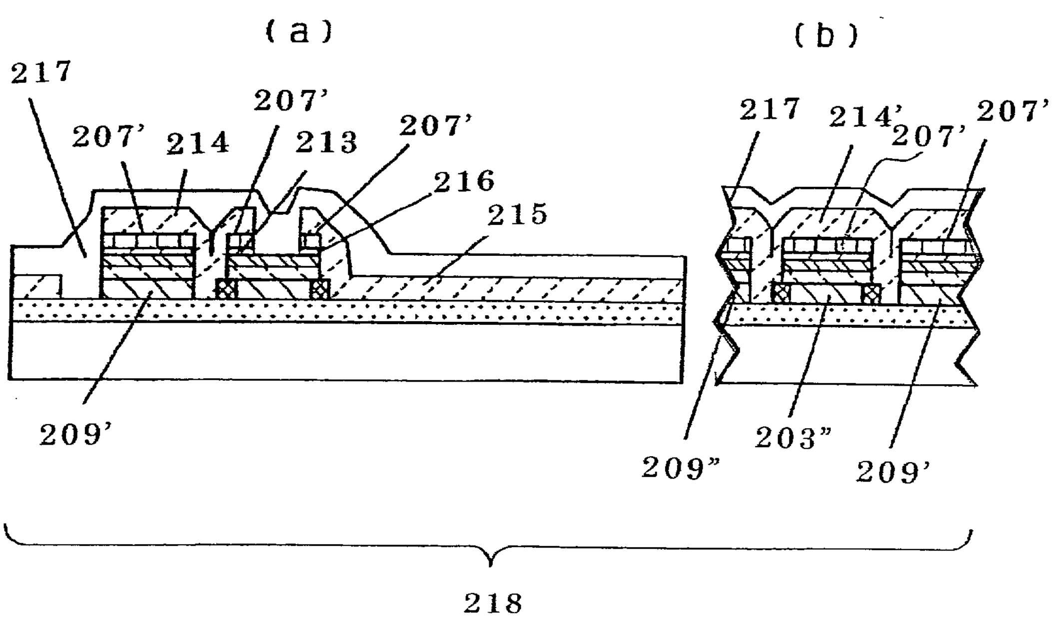
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Fig. 12

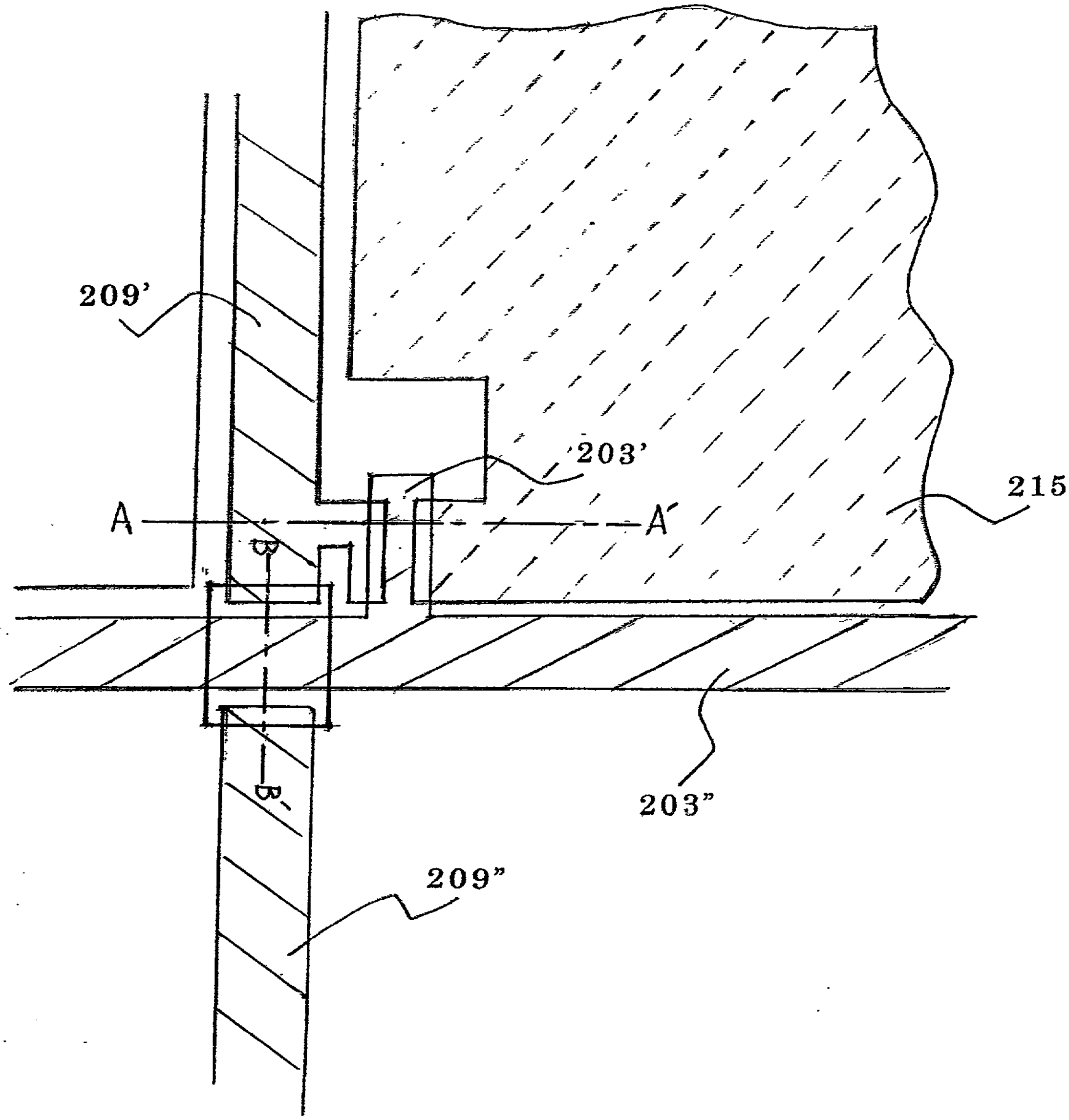

Fig. 13

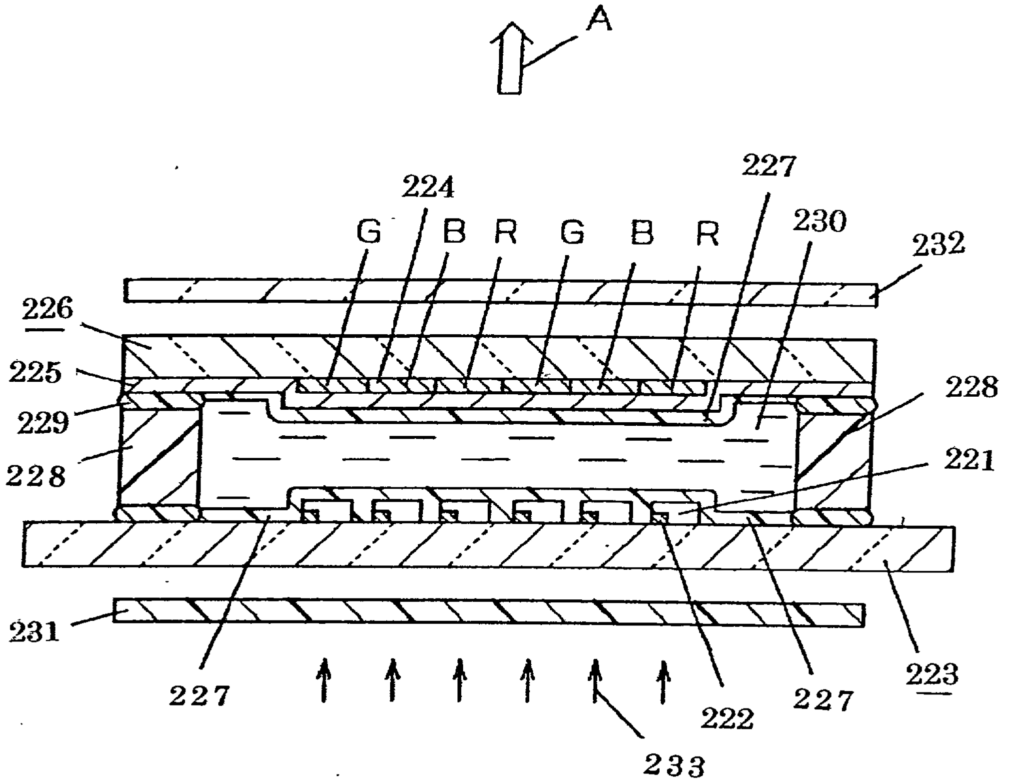
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Fig. 14

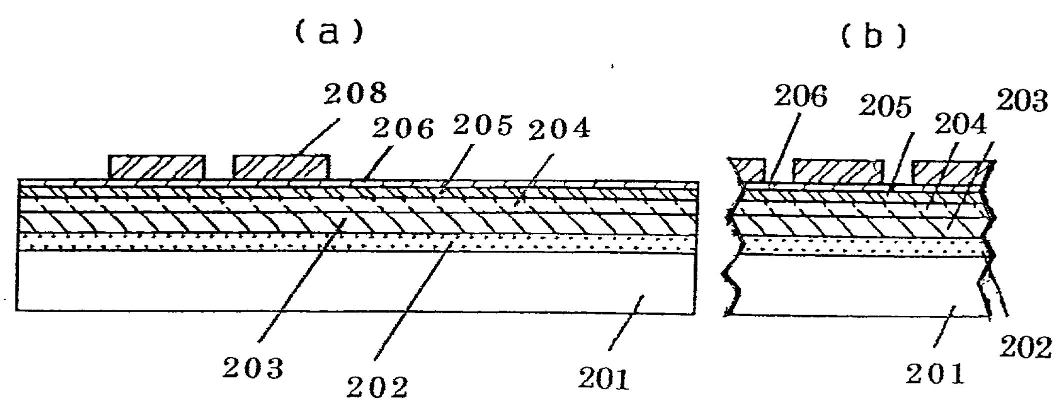
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Fig. 15

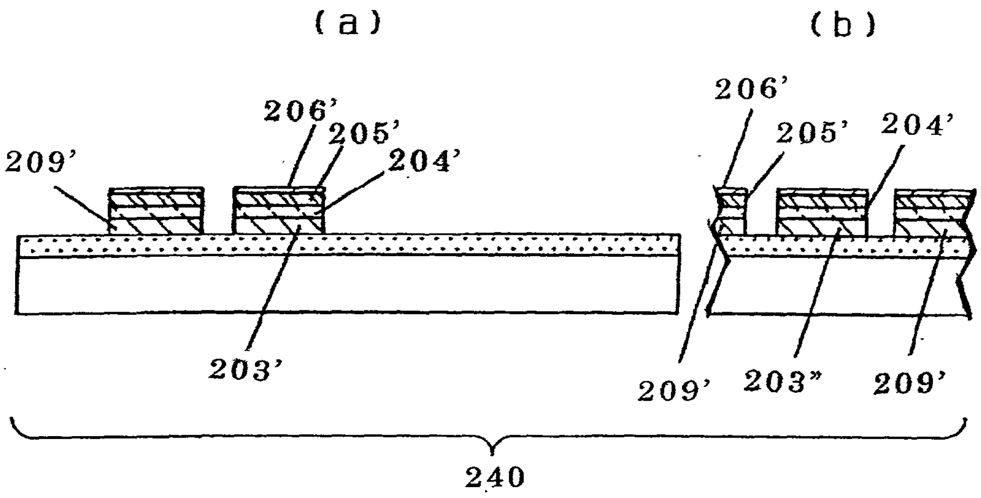

Fig. 16

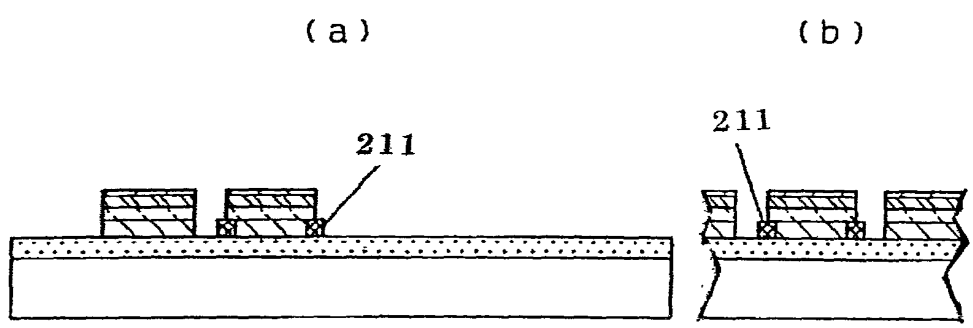

Fig. 17

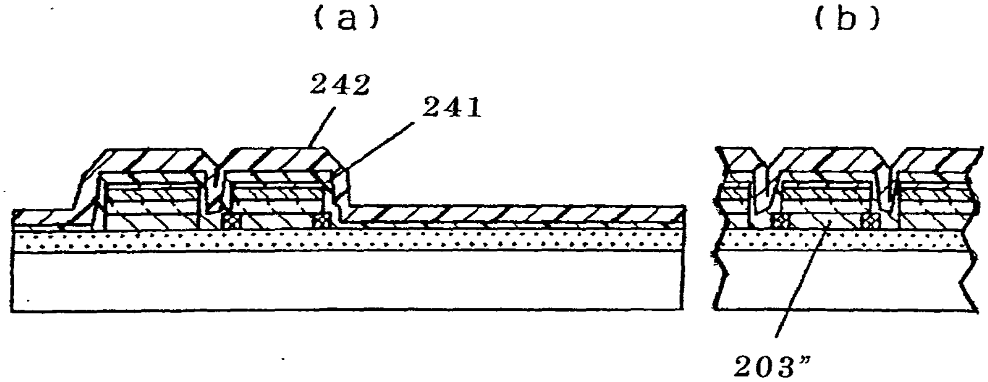

Fig. 18

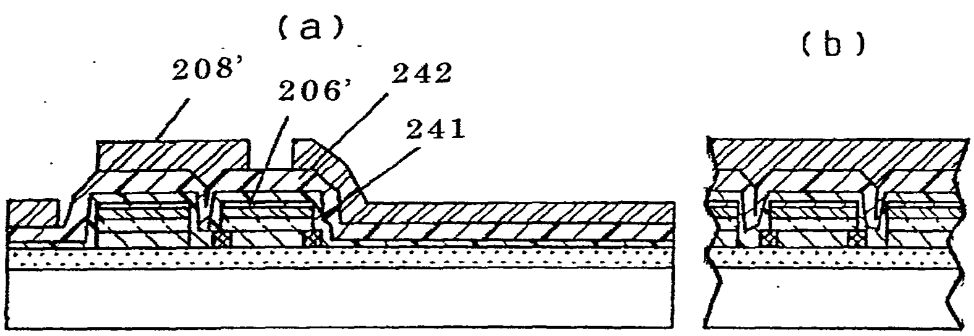

Fig. 19

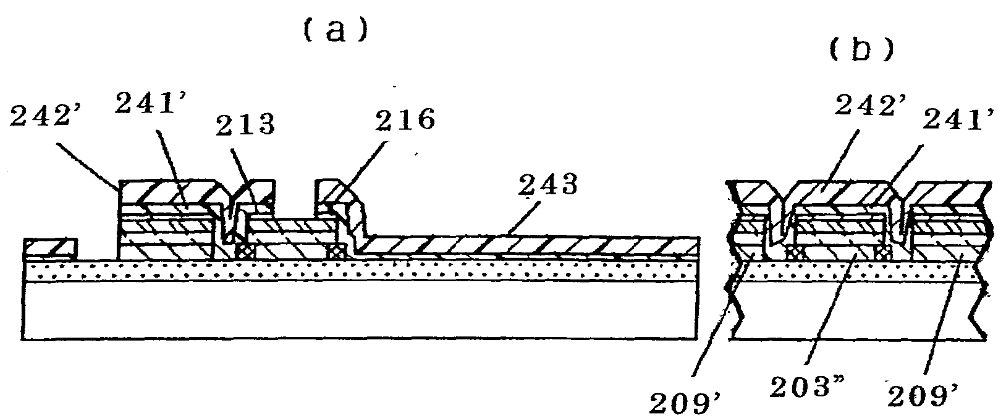

Fig. 20

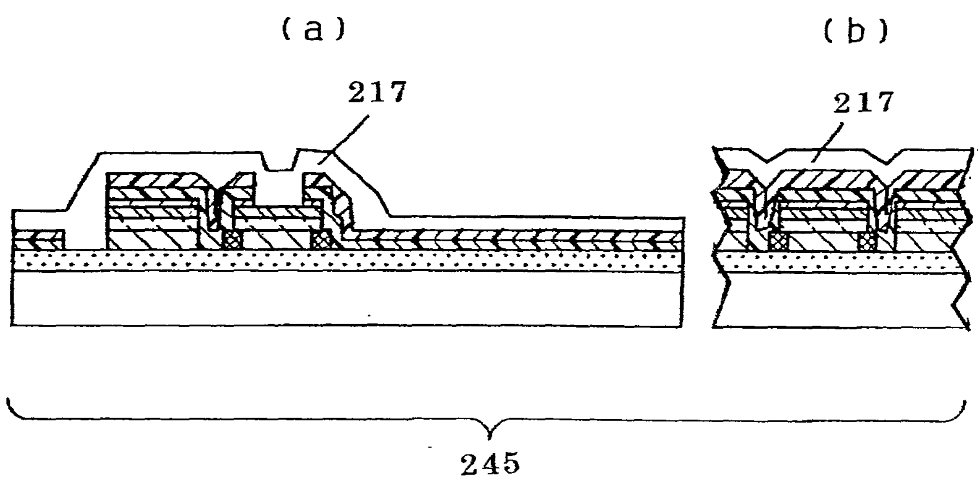

Fig. 21

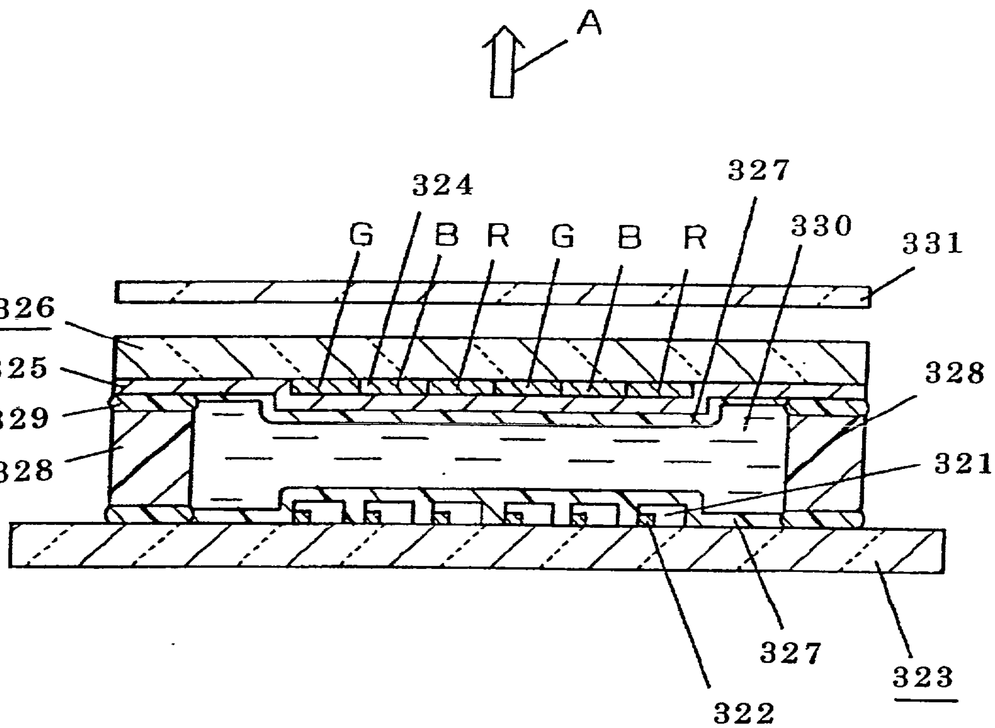
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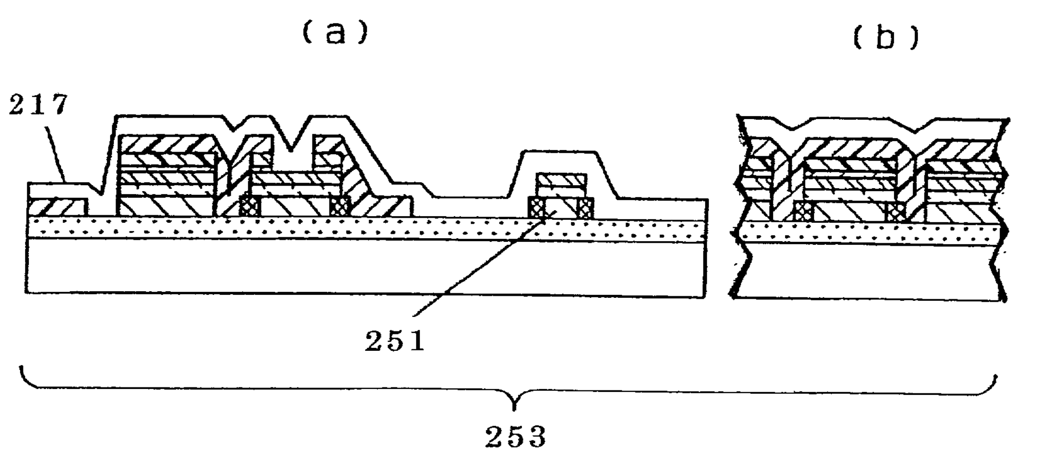
Fig. 22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(b)
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253

Fig. 23

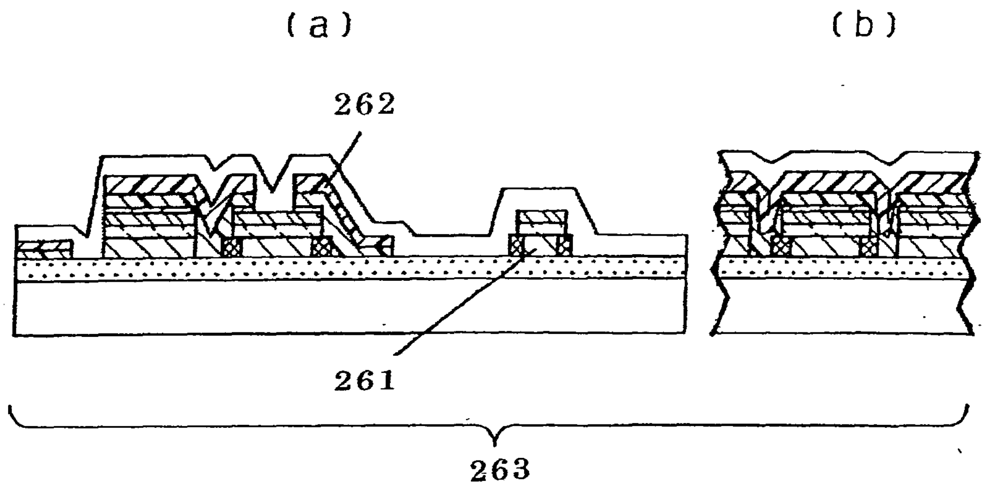


Fig. 24

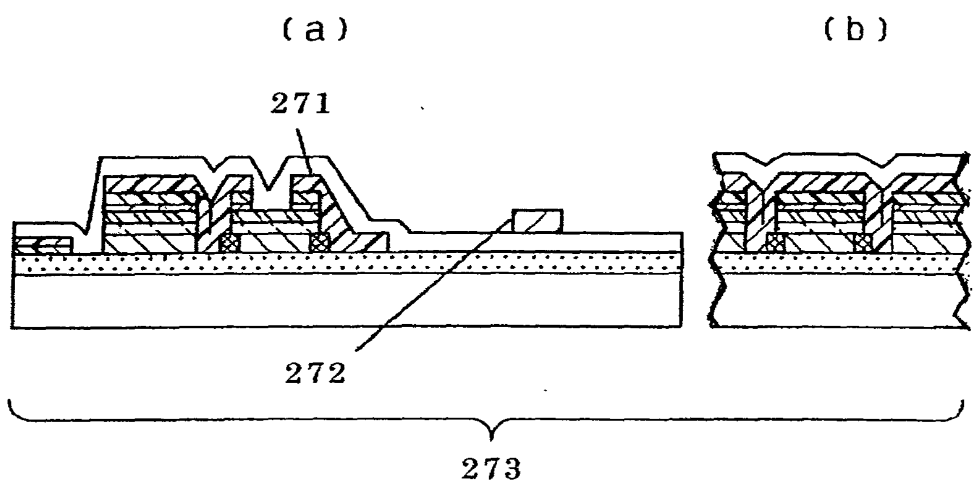


Fig. 25

(a) (b)

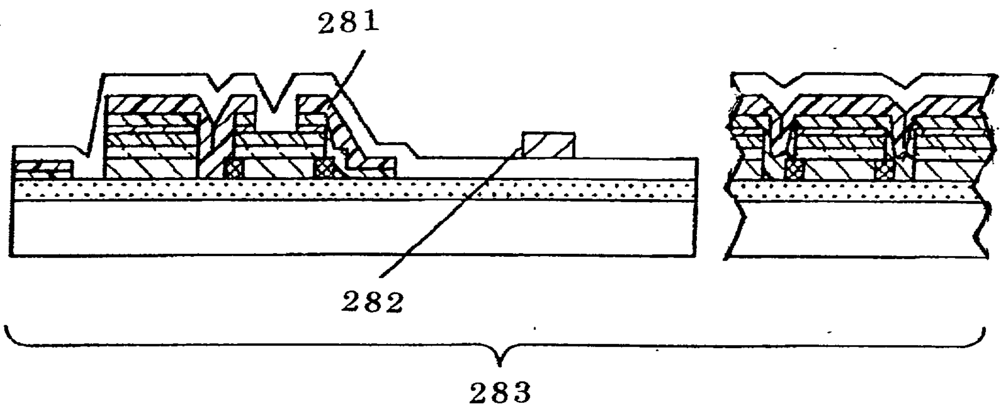
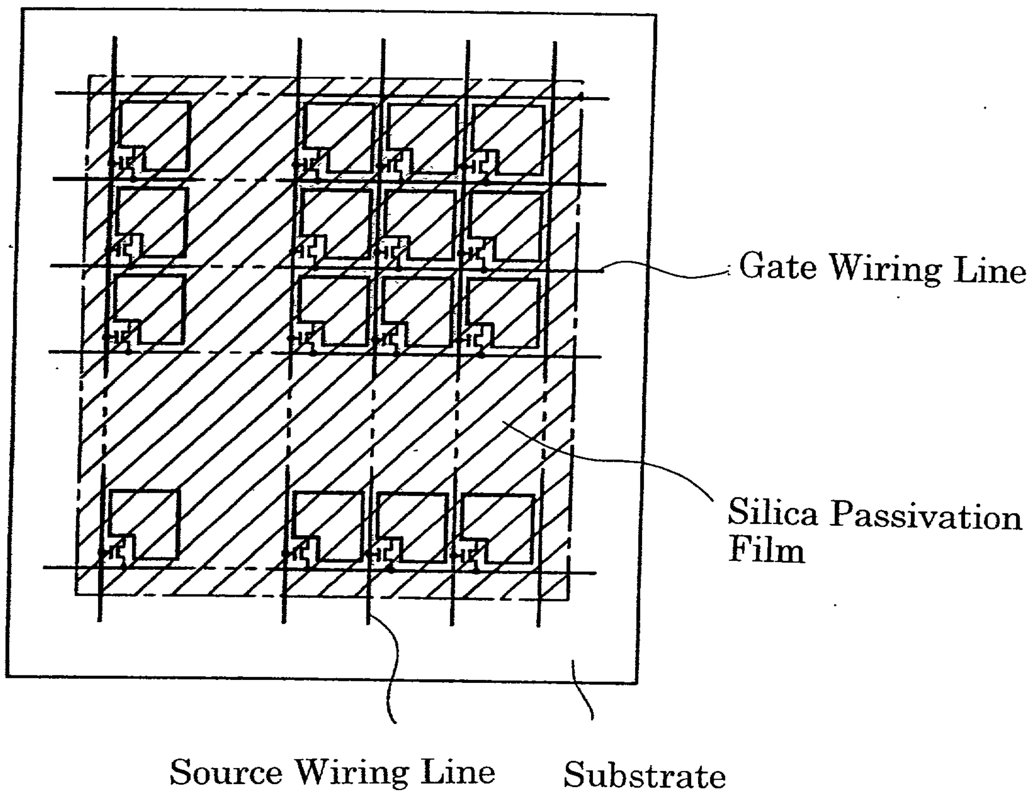


Fig. 26


Gate Wiring Line
Silica Passivation Film
Source Wiring Line
Substrate

Declaration and Power of Attorney Under Patent Cooperation Treaty 35 USC §371(c)(4)

As a below named inventor, I hereby declare that:

my residence, post office address and citizenship are as stated below next to my name; that

I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are named below) of the invention entitled: ELECTRICAL CIRCUIT BOARD AND TFT ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE UTILIZING THE SAME described and claimed in the international application number PCT/JP00/06173 filed September 8, 2000 and as amended on ______________ (if any), the specification and claims of which I have reviewed and understand and for which I solicit a patent.

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a), and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to my international application by me or my legal representatives or assigns, except as follows:

Japanese Patent Application No. H11-254385 filed on September 8, 1999

The priority of the above applications (if any), filed within a year prior to my international application is hereby claimed under 35 USC 119. I hereby appoint the following as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the patent office:

Roger W. Parkhurst, Reg. No. 25,177; Charles A. Wendel, Reg. No. 24,453; Lawrence D. Eisen, Reg. No. 41,009.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO: PARKHURST & WENDEL, L.L.P., 1421 PRINCE STREET, SUITE 210, ALEXANDRIA, VIRGINIA 22314-2805, TELEPHONE (703) 739-0220.

I hereby declare that I have reviewed and understand the contents of this Declaration, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

3. Full Name of Sole or First Inventor: Kazufumi (Given Name) — (Middle Initial) — OGAWA (Family Name)

1-W

*4. Inventor's Signature: Kazufumi Ogawa

Date of Signature: January (Month) 22 (Day), 2002 (Year)

6. Residence: Nara-shi (City), Nara (State or Province) SPX, JAPAN (Country)

7. Citizenship: Japanese

8. Post Office address (Insert complete mailing address, including country): 2-3-50, Aoyama, Nara-shi, Nara 630-8101 JAPAN

*IF THERE IS MORE THAN ONE INVENTOR USE PAGE 2 AND PLACE AN "X" HERE☐.